



Construction of a Power Electronics Cooling Test bed

Final Year Engineering Thesis, 2010

by

Markus Henke

01/10/2010

*A thesis submitted to the Department of Electrical and Mechanical Engineering in
partial fulfillment of the requirements as an exchange student.*

Synopsis

This thesis is the first part of the project to the subject: Construction of a Power Electronics Cooling Test Bed. In this project a test bed configuration for the evaluation of heat transfer characteristics for cooling power electronics devices and circuits is to be constructed. Heat generation based on power dissipation and switching speeds will be quantified using MOSFET power transistors, with possible extensions to more elaborate power electronic circuits. The goal is to produce a modular and robust testing apparatus to evaluate components and circuits at or above their published operating ranges for temperature. This thesis contains all important and essential information to the structure and operation of MOSFET power transistors as well as the first results of heat transfer measurements for different conditions. The future students of this project have a great introduction and important information for the further work on it.

Nativeness Statement

By setting my signature hereunder I explicate that this attached thesis is original and based upon my own, independent or in team accomplished intellectual work and no literal copy of prior released papers of a third, unless this is indicated in the text by reference.

Place, Date,

Signature

Acknowledgements

The author wishes to express his gratitude to the following individuals who contributed to making this final thesis possible:

First he would like to thank his supervisors Dr. Nathan B. Edgar at Arkansas State University, ing L.M.C. Muijtjens at Hogeschool Zuyd Heerlen and Prof. Dr.-Ing. Michael Trautwein at University of Applied Science in Aachen for their advice, encouragement, appreciation and assistance.

He also would like to thank Dr. Paul D. Mixon, Dr. Shivan Haran and Joe Murphy for supporting his work with their ideas, suggestions for improvements and the provided Hardware solutions at Arkansas State University.

A special thank goes to his assistant Steven Wehmeyer, a senior student of Mechanical Engineering, for his help and support with the experiment set-up and procedure of the measurements during this time.

Table of Contents

Synopsis	II
Nativeness Statement.....	III
Acknowledgements.....	IV
Table of Contents.....	V
List of Figures	VII
1 Introduction	1
1.1 Thesis Structure.....	1
2 Power MOSFET.....	2
2.1 Introduction.....	2
2.1.1 Output Characteristics.....	3
2.1.2 Safe Operating Area	4
2.2 Basic Structure.....	5
2.3 Static Electrical Characteristics.....	9
2.3.1 On-state Resistance.....	9
2.3.2 Drain-Source Breakdown Voltage	13
2.3.3 Gate Threshold Voltage.....	14
2.3.4 Zero Gate Voltage Drain Current and the Gate-Source Leakage Current....	15
2.4 Maximum Ratings.....	16
2.5 Dynamic Characteristics	21
2.5.1 Transconductance	22

2.5.2	Parasitic and Intrinsic Components.....	23
2.5.3	Intrinsic Capacitances.....	24
2.5.4	Gate Charge.....	27
2.5.5	Switching Operation.....	28
2.6	Temperature Effects.....	29
2.6.1	Switching Speed.....	30
2.6.2	Threshold Voltage.....	30
2.6.3	Transfer Characteristics.....	30
2.6.4	Breakdown Voltage.....	31
2.7	Thermal and Mechanical Characteristics.....	31
2.7.1	Thermal Model.....	33
3	Project Simulation.....	38
3.1	Heating a MOSFET Power Transistor.....	38
4	Project Measurements.....	41
4.1	Measurements without Enclosure.....	43
4.1.1	Upright Mounting.....	44
4.1.2	Side Mounting.....	49
4.2	Measurements with Aluminum Enclosure.....	54
5	Conclusion.....	60
6	References.....	61
	Appendix A.....	63

List of Figures

Figure 1: Output Characteristics, $T_C = 25^\circ\text{C}$	3
Figure 2: Output Characteristics, $T_C = 175^\circ\text{C}$	4
Figure 3: Maximum Safe Operating Area	5
Figure 4: Lateral N-Channel MOSFET Cross-Section.....	6
Figure 5: Vertical DMOS Cross-Section	7
Figure 6: VMOS Cross-Section	8
Figure 7: UMOS Cross-Section.....	9
Figure 8: Compounding of the on-state resistance.....	10
Figure 9: Relative Contributions to $R_{DS(ON)}$ for different voltage ratings	11
Figure 10: $R_{DS(ON)}$ vs Temperature.....	12
Figure 11: Power MOSFET Breakdown Characteristics	14
Figure 12: Maximum Drain Current vs. Case Temperature.....	17
Figure 13: Two possible Mechanism for dv/dt capability turn-on	20
Figure 14: Power MOSFET cross-section with parasitic components	23
Figure 15: Power MOSFET Structure Capacitances.....	25
Figure 16: Switching Waveforms for Resistive Load	28
Figure 17: Transfer Characteristics.....	31
Figure 18: Transient Thermal Impedance RC Model.....	32
Figure 19: Thermal Impedance “Family of Curves”	33
Figure 20: MOSFET Steady-State Thermal Resistance Model.....	33
Figure 21: Transient Thermal Resistance Model.....	35
Figure 22: Junction Temperature Response to a Step Pulse of Heating Power	36

Figure 23: top left – Heat Input; top right – Equivalent Heat Input by Superposition of Power Pulses; bottom left – Junction Temperature Response to Individual Power Pulse; bottom right – Use of Superposition to Determine Peak T_J	37
Figure 24: Train of Power Pulses	37
Figure 25: Screen Shot of Micro-Cap 9.....	38
Figure 26: Circuit for Heating the Power MOSFET	39
Figure 27: ID against V(V1) for different gate-source voltages.....	39
Figure 28: PD(MOSFET) against V(V1) for different gate-source voltages.....	40
Figure 29: LabVIEW Block Diagram for temperature measurements.....	41
Figure 30: LabVIEW Front Panel for temperature measurements.....	42
Figure 31: Experimental Set-up for measurements without enclosure.....	43
Figure 32: Set-Up Upright Mounting Side View.....	43
Figure 33: Set-Up Upright Mounting Top View.....	44
Figure 34: MOSFET Case Temperature (Upright Mounting)	45
Figure 35: Surrounding Temperature Effects 1mm Distance (Upright Mounting)	45
Figure 36: Surrounding Temperature Effects 2mm Distance (Upright Mounting)	46
Figure 37: Surrounding Temperature Effects 4mm Distance (Upright Mounting)	46
Figure 38: surrounding Temperature Effects 6mm Distance (Upright Mounting).....	46
Figure 39: Surrounding Temperature Effects 8mm Distance (Upright Mounting)	47
Figure 40: Surrounding Temperature Effects 10mm Distance (Upright Mounting)	47
Figure 41: Surrounding Temperature Effects beside the MOSFET (Upright Mounting)	48
Figure 42: Surrounding Temperature Effects in the Front of the MOSFET (Upright Mounting).....	48
Figure 43: Comparison Temperature versus Distance after 1000sec (Upright Mounting) .	49
Figure 44: Set-Up Side Mounting View 1.....	48
Figure 45: Set-Up Side Mounting View 2.....	49

Figure 46: MOSFET Case Temperature (Side Mounting).....	50
Figure 47: Surrounding Temperature Effects 1mm Distance (Side Mounting).....	50
Figure 48: Surrounding Temperature Effects 2mm Distance (Side Mounting).....	51
Figure 49: Surrounding Temperature Effects 4mm Distance (Side Mounting).....	51
Figure 50: Surrounding Temperature Effects 6mm Distance (Side Mounting).....	51
Figure 51: Surrounding Temperature Effects 8mm Distance (Side Mounting).....	52
Figure 52: Surrounding Temperature Effects 10mm Distance (Side Mounting).....	52
Figure 53: Surrounding Temperature Effects above the MOSFET (Side Mounting)	53
Figure 54: Surrounding Temperature Effects under the MOSFET (Side Mounting).....	53
Figure 55: Comparison Temperature versus Distance after 1000s (Side Mounting).....	54
Figure 56: Set-Up in enclosure (opened).....	53
Figure 57: Set-Up in enclosure (closed).....	54
Figure 58: MOSFET Case Temperature (aluminum enclosure)	55
Figure 59: Surrounding Temperature Effects 1mm Distance (Aluminum Enclosure)	55
Figure 60: Surrounding Temperature Effects 2mm Distance (Aluminum Enclosure)	56
Figure 61: Surrounding Temperature Effects 4mm Distance (Aluminum Enclosure)	56
Figure 62: Surrounding Temperature Effects 6mm Distance (Aluminum Enclosure)	56
Figure 63: Surrounding Temperature Effects 8mm Distance (Aluminum Enclosure)	57
Figure 64: Surrounding Temperature Effects in Front of the MOSFET (Aluminum Enclosure)	57
Figure 65: Surrounding Temperature Effects beside the MOSFET (Aluminum Enclosure) .	58
Figure 66: Comparison Temperature versus Distance after 1000s (Aluminum Enclosure)	59

1 Introduction

Heat transfer, mostly caused by power dissipation and switching speed, is a very important and exasperating topic in electronic devices. Too much heat can cause catastrophic failures or even the destruction of the device. Therefore the knowledge about heat transfer characteristics of the used electronic components is an essential basis for developing electronic circuits. According to this a test bed for cooling of power electronics would be a helpful device for discovering the heat transfer characteristics of an electronic component.

1.1 Thesis Structure

This thesis is divided into two main and independent parts: chapter 2 and chapter 3 and 4.

Chapter 2 is about the structure and operation of a MOSFET power transistor by way of example for an electronic component. More precisely, in this thesis the MOSFET power transistor IRLZ14 is used and thus all figures are referred to this type of transistor.

Chapter 3 and 4 are about the procedure for the practical measurement of heat transfer characteristics. This procedure is divided into the simulation and the measurements it selves.

The paper ends with a final conclusion, including a summary of all found characteristics and distinctive features.

2 Power MOSFET

2.1 Introduction

A Power MOSFET is a specific type of a MOSFET, a metal oxide semiconductor field-effect transistor, which is developed to handle large power. Its invention was partly driven by the limitations of bipolar power junction transistors (BJTs). The main advantages are the high communication and switching speed, which is several times faster than bipolar power junction transistors of similar size and voltage rating, the very good efficiency at low voltages and because of its insulated gate, only very little gate drive power is necessary and so it is easy to drive. For these reasons a Power MOSFET approaches characteristics of an ideal switch. In principle a Power MOSFET works with the same operating principle like a “normal” MOSFET, but you talk about power devices, if this device can switch at least 1A current. It is most widely used as a low-voltage switch, which means 200V, and below, and in power supplies or DC to DC converter.

There are two main reasons, why the Power MOSFET rejoices in ever increasing popularity. The first is its high input impedance and the second reason is that it is a majority carrier device, which means that these devices do not suffer from minority carrier storage time effects, thermal runaway or a second breakdown. Its main drawbacks are the on-resistance $R_{DS(on)}$ and the strong positive temperature coefficient, but the advantages against bipolar power junction transistors preponderate. These are:

- Superior switching speed
- Less switching power losses in high frequency applications
- No second breakdown (withstand of higher current and voltage in simultaneous applications)
- Even distribution of current when paralleled, because forward voltage drop increases with increasing temperature

2.1.1 Output Characteristics

An important feature in the MOSFET characterization is the output characteristics (Figure 1 + 2). This feature is shown in graph I_D vs. V_{DS} and in the majority of cases released in the datasheet of the MOSFET, often for two different case temperatures T_C .

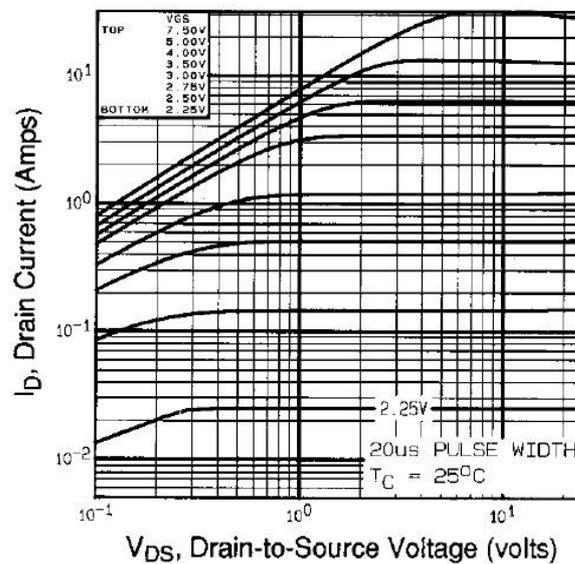


Figure 1: Output Characteristics, $T_C = 25^\circ\text{C}$

This graph shows two distinct regions of operation, the “linear” and the “saturated” region. To understand the difference between these two regions you need to look at the current path inside of the MOSFET. This path is first horizontal under the gate oxide and then vertical through the drain. In the “linear” operation region the voltage across the MOSFET channel is not sufficient enough for carriers to reach their maximum current density. So the on-resistance is constant and defined as:

$$R_{DS(ON)} = \frac{V_{DS}}{I_{DS}}$$

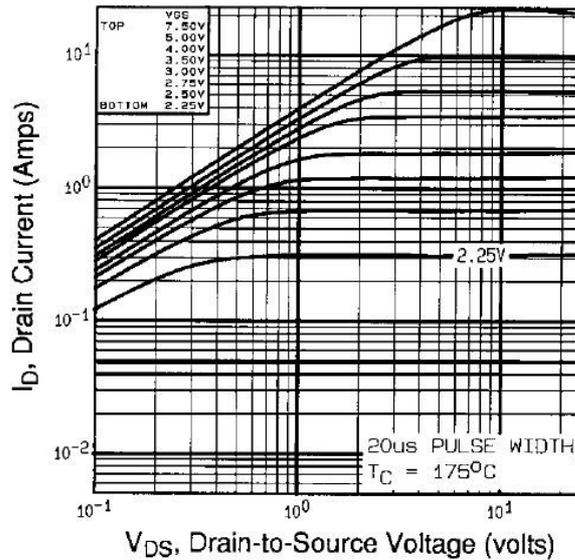


Figure 2: Output Characteristics, $T_C = 175^\circ\text{C}$

In the “saturation” region V_{DS} increases and the carriers reach their maximum drift velocity. The current amplitude cannot increase and the device is now behaving like a current generator and therefore with a high output impedance.

2.1.2 Safe Operating Area

The safe operating area is a function of current and voltage which are applied to the device. It is graphically represented as a plot of current vs. voltage within the “safe” area is shown. It defines the combined ranges of drain current and drain to source voltage the MOSFET can handle without damage. The drain current and the drain to source voltage must stay below their maximum values as well as their product has to stay below the maximum power dissipation the MOSFET can handle.

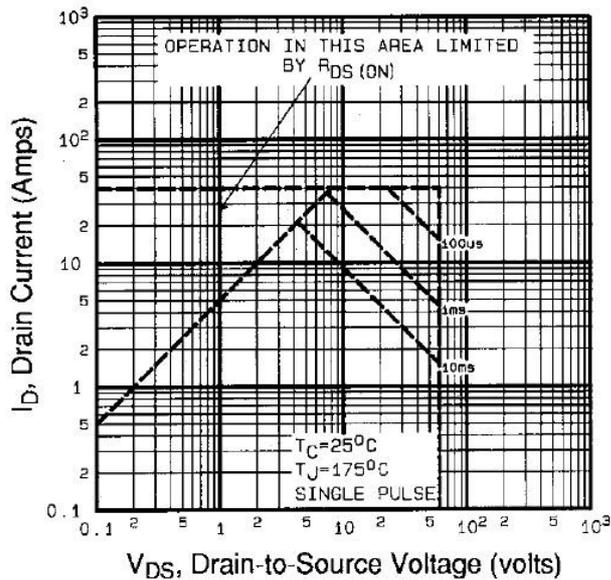


Figure 3: Maximum Safe Operating Area

One of the most important advantages of Power MOSFETs against bipolar transistors is that no forward or bias second breakdown can occur when the transistor turns on or off. This is caused by thermal hot spots in the silicon. In a Power MOSFET the carriers travel through the device as it were a bulk semiconductor, which exhibits a positive temperature coefficient. If the current now tries to self constrict to a localized area the temperature of the spot will increase, which will raise the spot resistance due to the positive temperature coefficient of the bulk silicon. So the higher voltage drop will be aimed at reallocating the current from the hot spot.

2.2 Basic Structure

There are two basic structures in the MOSFET technology, the lateral and the vertical structure. Power MOSFET are for several reasons mainly manufactured with a vertical structure, but for understanding the operation of MOSFETs it is suggestive first to consider the lateral N-Channel MOSFET shown in Figure 4.

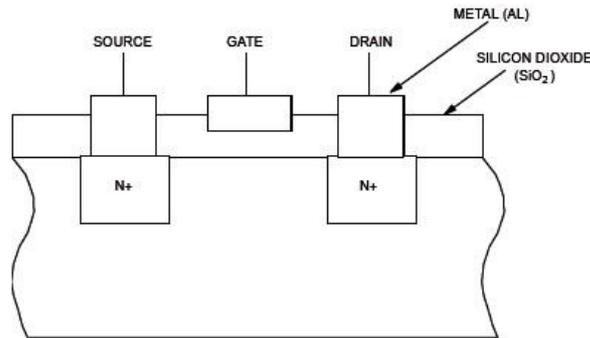


Figure 4: Lateral N-Channel MOSFET Cross-Section

If there is no electrical bias applied to the gate, there is a blocking PN junction underneath the gate, so that no current can flow. When both a forward gate-source voltage and a drain-source voltage is applied the free hole carriers in the p-epitaxial layer are repelled away from the gate, which creates a channel in which electrons can flow from source to drain. For this reason electrons are the majority carriers in a MOSFET and this is also the reason why this operation mode is called “enhancement”, which means it is normally “off”. The opposite operation mode is called “depletion” and is by contrast a so called “on” device. In a lateral structure, the current and breakdown voltage ratings are both functions of the channel dimensions width and length.

As advantage of the lateral MOSFET structure the low gate signal power requirement, which is caused by the gate oxide capacitance can be mentioned. When this capacitance has charges, no gate current can flow into the gate any longer. Another advantage is the fast switching speed, because as soon as the channel is created the electrons will flow. There are also no storage time effects like in transistors, since the channel depth is proportional to the gate voltage and so the pinches close as soon as the gate voltage is removed. The major disadvantage of the lateral MOSFET structure is the high resistance channel. The source is electrically connected to the substrate, with no gate bias the depletion region extends out from the N^+ drain in a pseudo hemispherical shape, so that the minimum depletion width which is required to support the rated voltage of the device affects the minimum channel lengths. This problem may be decreased by wider channels, but this not

only costly; it would be a good deal increasing the gate capacitance and thus slow down the switching speed of the device.

The Power MOSFET structure is like mentioned above in most cases a vertical structure and therefore one is also talking about the Vertical Diffused MOS (VDMOS) or Double Diffused MOS (DMOS) and is shown in Figure 5.

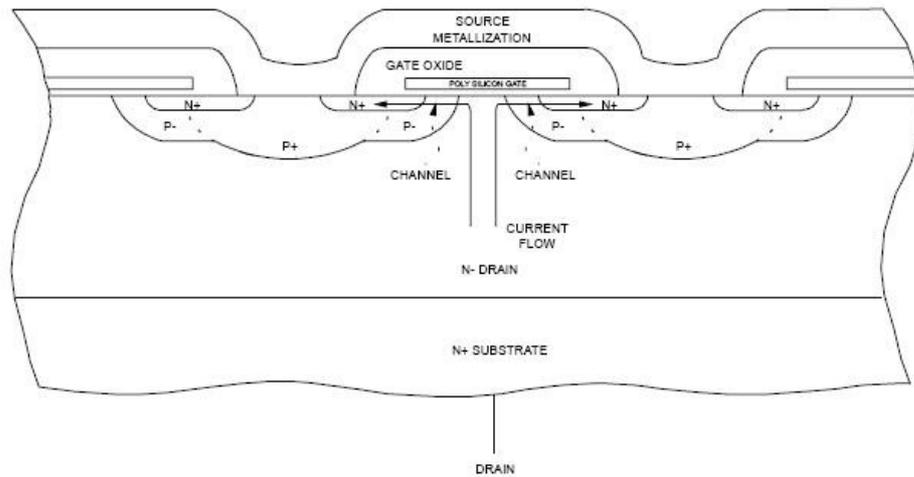


Figure 5: Vertical DMOS Cross-Section

In this structure the source electrode is placed over the drain, which causes a vertical current flow when the MOSFET is on-state. The current path is created by inverting the p-layer under the gate. This takes place in the identical method like the in lateral MOSFETs. The current flows first horizontally under the gate and then vertically through the drain. A MOSFET with this structure consists of thousands paralleled N^+ sources, which result in a lower on-resistance for the same blocking voltage and also faster switching speed. The diffusion in a VDMOS refers to the manufacturing process in which the P wells are obtained by a diffusion process. Actually it is a double diffusion process to get the P and N^+ regions. Thus the name double diffused MOSFET.

With a positive gate-source voltage V_{GS} , the electrons are drawn toward the gate in the body region. If the gate-source voltage reaches the so called threshold voltage enough electrons are accumulate underneath the gate to create an inversion n-type layer and so a conductive channel across the body region. The MOSFET now is enhanced. In this state electrons can flow in either directions

through the channel. Talking about the positive or forward drain current means moving the electrons from source to drain. This forward drain current is blocked hence once the channel is turned off and the drain-source voltage is supported by the reverse biased body-drain PN junction. In a vertical structure the voltage rating is a function of the doping and thickness of the N epitaxial layer and the current rating is a function of the channel width. This sustains high blocking voltage and high current within a compact piece of silicon. This design is configured for switching applications due to their high switching speed and low switching losses.

In the vertical structure different kinds of build-up exist. The most commons are the VMOS (Figure 6), which has a V-groove at the gate region and was the first commercial device, the UMOS (Figure 7), where the gate electrode is buried in a U-shaped trench etched in the silicon. This results in a vertical channel and the main advantage is the absence of the parasitic JFET effect, which is described later in this paper. The third build-up is the CoolMOS, which is especially designed for voltages beyond 500V.

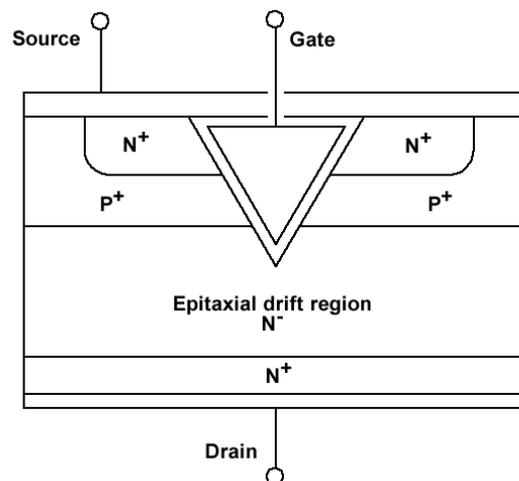


Figure 6: VMOS Cross-Section

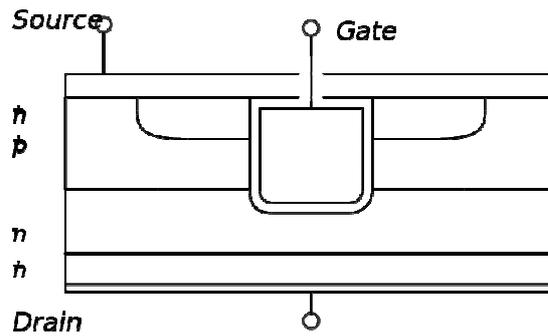


Figure 7: UMOS Cross-Section

In addition to this vertical construction design many source geometries are possible, for example squares, triangles, hexagons, etc. There are many considerations that determine the source geometry: the on-resistance, the input capacitance, the switching times and the transconductance.

2.3 Static Electrical Characteristics

By viewing the special characteristics of a Power MOSFET, you have to distinguish between dynamic and static characteristics. In both cases several important characteristics describe the Power MOSFET in this state. In the further course of this thesis static electrical characteristics are equalized with on-state characteristics.

2.3.1 On-state Resistance

The on-state resistance $R_{DS(ON)}$ characterizes the resistive behavior between the drain and the source terminals at a specified drain current (usually 0.5 times of the maximum continuous drain current I_D) and gate-source voltage (usually 10V) at a temperature of 25°C. It is a sum of many elementary contributions and is defined as

on-state voltage divided by on-state current. It also determines how much current the device can carry for low to medium frequencies (< 200kHz), the power loss and heating.

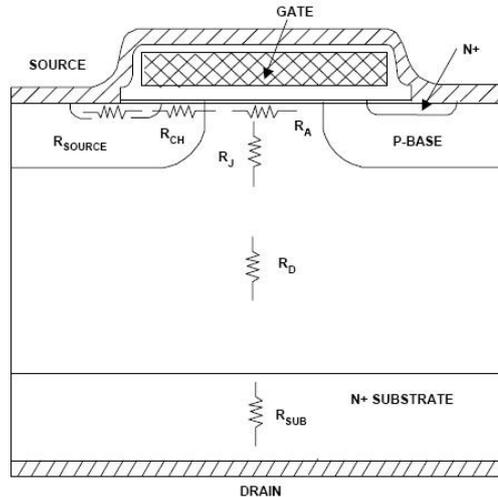


Figure 8: Compounding of the on-state resistance

As you can see in figure 8, the on-state resistance is a series connection of several components and results in the following equation:

$$R_{DS(ON)} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml}$$

Where:

R_{source} : Source resistance

R_{ch} : Channel resistance (directly proportional to the channel width and for given die size to channel density)

R_A : Accumulation resistance (resistance of epitaxial zone under the gate electrode → change from horizontal to vertical current direction)

R_J : “JFET” component resistance (of region between the two body regions → P implantations form the gate of a parasitic JFET transistor that tend to reduce the width of the current flow)

R_D : Drift region resistance (resistance of the epitaxial layer, which is directly related to the voltage rating. High voltage: thick layer → low-doping level → highly resistive. Low voltage: thin layer → high-doping level → less resistive)

R_{sub} : Substrate resistance (resistance of the N^+ substrate)

R_{wcmf} : Sum of Bond Wire resistance, Contact resistance between source and drain Metallization and the silicon, metallization and Lead frame contributions.

Addicted to the applied voltage to the MOSFET different components inside dominate the total resistance of the MOSFET. This is at high voltages the Epitaxial resistance and the JFET component and at low voltages the channel resistance and the contributions from metal to semiconductor contact, the metallization, the band wires and the lead frame.

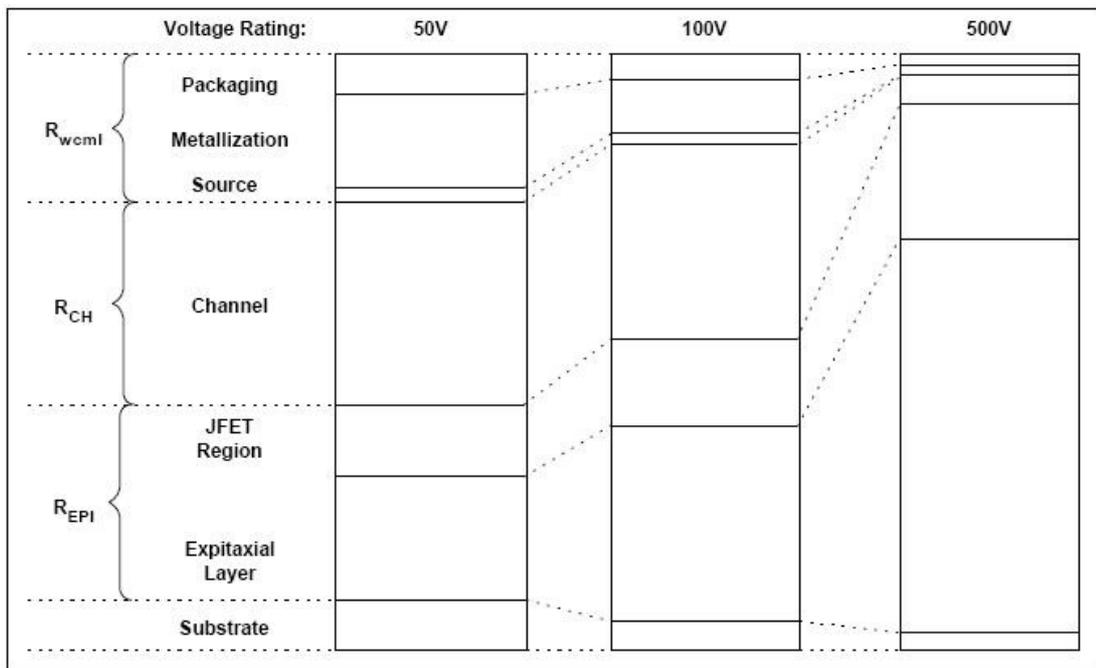


Figure 9: Relative Contributions to $R_{DS(ON)}$ for different voltage ratings

The on-state resistance can be affected by different parameters, like current or temperature. The current effect is relatively weak, doubling of the current just results in about 6% increase in $R_{DS(ON)}$, the temperature on the other hand has a strong effect. For example $R_{DS(ON)}$ approximately doubles from 25°C to 125°C as you can see in Figure 10. $R_{DS(ON)}$ is according to this a function of T_j and hence it has different values for different temperatures. In this graph you can also see, that the temperature coefficient is always positive, because it is shown as the slope of the curve and this is because of the majority-only carriers. This strong positive temperature coefficient compounds the $I^2 \times R^2$ conduction losses as temperature increases. On the other hand, this positive temperature coefficient is practical when

paralleling Power MOSFETs, because it ensures thermal stability. The reason for the relatively easiness of paralleling is the relatively narrow part-to-part parameter distribution combined with the security from current hogging, which is provided by the positive temperature coefficient. If there is any imbalance between MOSFETs this does not result in current hogging because the device with the most current heat up and the higher on-voltage will divert the current to the other devices in parallel.

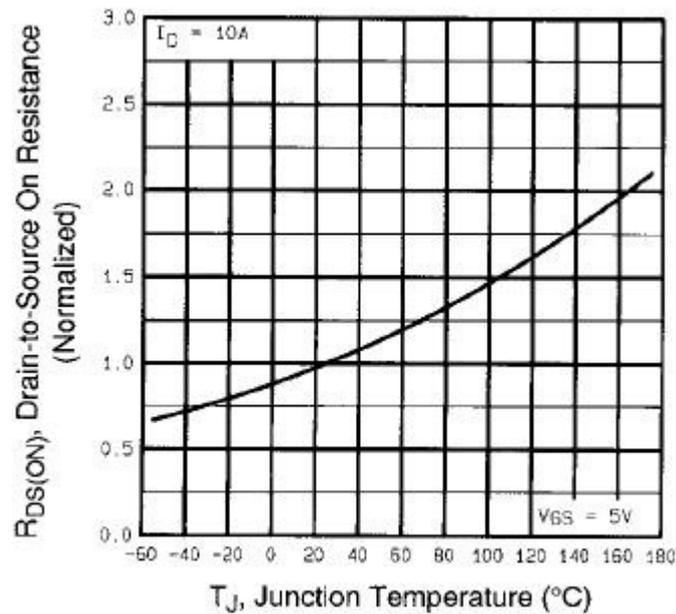


Figure 10: $R_{DS(ON)}$ vs Temperature

As you can see, the on-state resistance is one of the most important characteristics for power loss of the device. The lower $R_{DS(ON)}$ the lower the device power loss the cooler it will operate. A low $R_{DS(ON)}$ also reduces the heat sinking requirements and hence it lowers the parts and assembly costs. It can also eliminate the need to parallel MOSFETs and improves reliability. The on-state resistance decreases with increasing cell density, which is today around 12 million and higher per square inch for Power MOSFETs in trench technology.

2.3.2 Drain-Source Breakdown Voltage

The drain-source breakdown voltage $V_{(BR)DSS}$ is this drain-source voltage when no more than the specified drain current (normally 250 μ A) will flow at a specified temperature and the gate-source voltage is zero. At this voltage the reverse-biased body-drift diode breaks down and current can flow between source and drain. If the drain voltage is smaller than $V_{(BR)DSS}$ and no bias is on the gate, no channel will be created under the gate at the surface. The drain voltage is supported by the reverse-biased body-drift PN junction. Because of the positive temperature coefficient of a Power MOSFET, it can block more voltage when it is hot. If the MOSFET is cold the drain-source breakdown voltage is less than the maximum drain-source voltage V_{DSS} rating at 25°C.

You have to distinguish between the off-state and the on-state mode of a MOSFET, because the performance of the MOSFET varies for each mode. In the MOSFET off-state, it is equivalent to a PIN diode, which is constituted by a P⁺ diffusion, an N⁻ epitaxial layer and an N⁺ substrate. This structure is highly non-symmetrical and if this structure is reverse-biased the space-charge region extends principally on the light-doped side, which is normally the N⁻ layer. This layer has to withstand most of the off-state drain-source voltage. The performance in on-state mode on the other hand is different. Here the N⁻ layer has no function and beyond this its intrinsic resistivity as a lightly-doped region is non-negligible and has to be added to the on-state resistance. So two main parameters govern both the breakdown voltage and the on-state resistance. This is on the one hand the doping level and on the other hand the thickness of the N⁻ epitaxial layer. The thicker the layer and the lower its doping level, the higher is the breakdown voltage and the thinner the layer and higher its doping level, the lower is the on-resistance and therefore the lower the conduction losses of the MOSFET.

Two related phenomena may occur in Power MOSFET devices: punch-through and reach-through. When talking about a punch-through the depletion region on the source side of the body-drift PN junction reaches the source region at a drain

voltage below the rated avalanche voltage of the device. If this happens a current path between source and drain is created and it will cause a so called soft breakdown as shown in Figure 11. A leakage current is flowing between source and gate which is denoted by the drain current at zero gate voltage I_{DSS} . So trade-offs have to be made between the on-state resistance and punch-through avoidance.

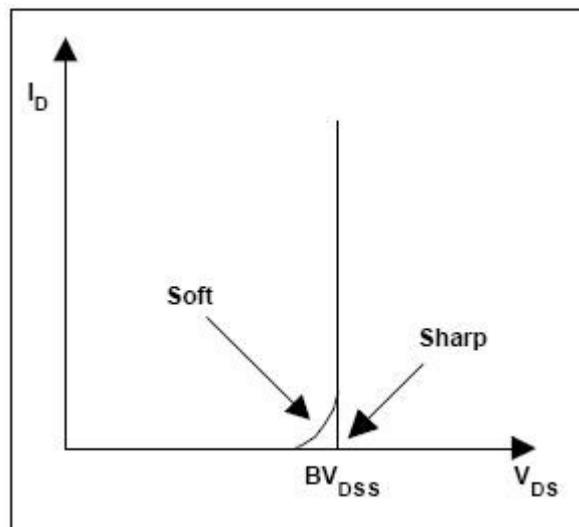


Figure 11: Power MOSFET Breakdown Characteristics

Does the on-state resistance require shorter channel lengths, so does punch-through avoidance requires longer channel lengths. The second possible phenomena, the reach-through, can occur when the depletion region on the drift side of the body-drift PN junction reaches the epitaxial layer substrate interface before avalanche takes place in the epitaxial layer. This brings a further increase of the drain voltage which is responsible for the fast achievement of the critical value of 2×10^5 V/cm of the electric field, where avalanching begins.

2.3.3 Gate Threshold Voltage

The gate threshold voltage or only threshold voltage $V_{GS(th)}$ describes this gate-source voltage at which the drain current begins or stops flowing. It is the minimum gate electrode bias which is needed to invert the surface under the gate and form a

conducting channel between drain and source. This value varies between each device and for this reason a range is specified in $V_{GS(th)}$ with minimum and maximum values. These values represent the edges of the $V_{GS(th)}$ distribution. It is usually measured at a drain-source current of $250\mu A$. The threshold voltage has a negative temperature coefficient, which means if the device heats up it will turn on at a lower gate-source voltage. A common $V_{GS(th)}$ value for high voltage devices is 2 – 4V and for low voltage devices 1 – 2V. For Power MOSFETs only a high value for $V_{GS(th)}$ is used, because a low value is undesirable for several reasons. The first one is like mentioned above the decreasing value for increasing temperature. Furthermore the high gate impedance makes it susceptible to spurious turn-on due to gate-noise and because of a thinner gate oxide for lower $V_{GS(th)}$ values, which lowers the gate oxide rating and can again cause a gate-oxide voltage punch-through.

2.3.4 Zero Gate Voltage Drain Current and the Gate-Source Leakage Current

Two more static electrical characteristics of a Power MOSFET are the zero gate voltage drain current I_{DSS} and the gate-source leakage current I_{GSS} . I_{DSS} is defined as the drain-source leakage current at a specified drain-source voltage when the gate-source voltage is zero. This value increases with the temperature of the device and is therefore specified at low temperature and when it is hot. The leakage power loss is calculated by the multiplication of I_{DSS} with the drain-source voltage and is usually negligible.

The gate-source leakage current in contrast is defined as the leakage current through the gate at a specified gate-source voltage.

2.4 Maximum Ratings

Each device and therefore the Power MOSFET too, has specified maximum ratings which must not exceed by operating. Their values are mostly specified in the datasheets of the device. In this chapter you can find a short overview about the most important maximum ratings with a small description.

- **V_{DSS} – Drain-Source Voltage**

The maximum drain-source voltage without causing avalanche breakdown, when the gate is shorted to the source at a case temperature T_C of 25°C.

- **V_{GS} – Gate-Source Voltage**

The maximum voltage between gate and source beyond breakdown may occur. This rating should prevent damage of the gate oxide. Exceeding of this value can cause turn on and so potentially damage the device and often other circuit elements. This also causes excessive power dissipation.

- **I_D – Continuous Drain Current**

The maximum continuous DC current with the die at the maximum rated junction temperature $T_{J(max)}$ and the case temperature T_C at 25°C. This rating is below the certain specified value and thus higher values can be reached for a very short time. I_D is based on the junction to case thermal resistance $R_{\Theta JC}$ and the case temperature T_C .

$$P_D = \frac{T_{J(max)} - T_C}{R_{\Theta JC}} = I_D^2 \cdot R_{DS(on)} @ T_{J(max)}$$

$\frac{T_{J(max)} - T_C}{R_{\Theta JC}}$ is the maximum heat that can be dissipated and equals the maximum allowable heat, that is generated by conduction loss $I_D^2 \cdot R_{DS(on)} @ T_{J(max)}$.

From this it follows, that:
$$I_D = \sqrt{\frac{T_{J(max)} - T_C}{R_{\theta JC}} \cdot \frac{1}{R_{DS(on)} @ T_{J(max)}}}$$

The drain current establishes the ability to drive a specific load, but can be limited by the package and by heating due to resistive losses in internal components. If you use the MOSFET in a pulsed mode the drain current can be several times the MOSFET's continuous rating. In the datasheets of MOSFET transistors the continuous drain current is always shown as a function of the case temperature T_C . It shows I_D over a range of case temperatures, but switching losses are not included.

The package leads of a MOSFET can also limit the maximum continuous current, there is for the TO-247 and TO-264 package a limit of 100 A, for the TO-220 package a limit of 75A and for the SOT-227 package a limit of 220A.

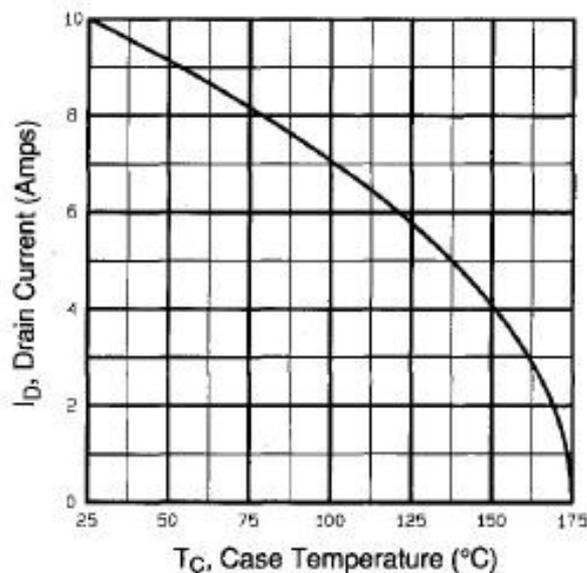


Figure 12: Maximum Drain Current vs. Case Temperature

- **I_{DM} – Pulsed Drain Current**

The value I_{DM} describes how much pulsed current the device can handle and is significantly higher than the maximum continuous drain current, at which the pulse width and duty cycle determine the safe drain current on device power

dissipation. There are three different purposes of the I_{DM} rating. The first one is to keep the MOSFET operating in the ohmic region. There is a maximum drain current for a corresponding gate-source voltage therefore. Is the operating point at a given gate-source voltage above the ohmic region “knee”, a further increase in drain current would result in a significant rise in drain-source voltage with a consequent rise in conduction loss. Is the power dissipation too high for too long the device will fail and therefore the I_{DM} rating is set below “knee”. The second purpose is to limit the current density to prevent die heating. Otherwise it may result in a burnout site and the third one is to avoid problems with excessive current through bad wires.

For thermal limitations the temperature rise depends upon the pulse width, the time between the pulses, the heat dissipation and the on-state resistance as well as the shape and the magnitude of the current pulse.

- **P_D – Power Dissipation**

P_D is the maximum power that the device can dissipate based on the maximum junction temperature (normally between 150°C and 175°C) and the thermal resistance $R_{\Theta JC}$ at a case temperature of 25°C. It is the maximum allowable power dissipation that will raise the die temperature to its maximum allowable.

$$P_D = \frac{T_{J \max} - T_C}{R_{\Theta JC}}$$

- **Maximum Temperature**

It is very important that the junction temperature of the MOSFET stays under a specified maximum value for the device to ensure a reliable function. First of all the packaging often limits the maximum junction temperature, due to the molding compound and epoxy characteristics. The power dissipation and the thermal resistance determine the maximum operating ambient temperature and the junction-to-case thermal resistance is intrinsic to the device and package. The case-to-ambient thermal resistance in contrast is largely dependent on the board/mounting layout, heat sinking area and air/fluid flow.

The maximum operating temperature is mostly affected by the type of power dissipation, whether it is continuous or pulsed, due to thermal capacitance characteristics. The lower the frequency of pulses for a given power dissipation, the higher the maximum operating ambient temperature. So it allows a longer interval for the device to cool down.

- **E_{AS} – Single Pulse Avalanche Energy**

Leakage and stray inductances can cause a voltage overshoot and this overshoot can exceed the breakdown voltage of a device. If this overshoot does not exceed the breakdown voltage the device will not avalanche and thus it does not need to dissipate avalanche energy. If a device is avalanche energy rated, which means it offers, depending on the amount of energy dissipated in avalanche mode, a safety net for over-voltage transients, it has an E_{AS} rating. This indicated how much reverse avalanche energy the device can safely absorb.

$$E_{AS} = \frac{L \cdot i_D^2}{2}$$

(L = value of an inductor carrying a peak current i_D , which is suddenly diverted into the drain of the device under test)

An avalanche condition allows the inductor current to flow through the MOSFET, even though the MOSFET is off-state. Energy stored in the inductor is analogous to energy stored in leakage and/or stray inductances and is dissipated in the MOSFET.

- **dv/dt Capability**

Dv/dt capability is defined as the maximum rate of rise of drain-source voltage allowed. If this rate is exceeded the gate-source voltage may become higher than the threshold voltage of the device and this forces the device into current conduction mode what can create a catastrophic failure under certain conditions. There are two possible mechanisms by which a dv/dt capability induced turn-on can take place. The first one is the feedback action of the gate-

drain capacitance C_{GD} . This capacitance forms together with the gate-source capacitance a capacitance divider, which can generate a pulse sufficient to exceed the threshold voltage. If there is a voltage ramp across drain and source a current I_1 flows through the total gate resistance R_G by dint of the gate-drain capacitance. The voltage drop across is R_G is:

$$V_{GS} = I_1 \cdot R_G = R_G \cdot C_{GD} \frac{dv}{dt}$$

If the gate voltage exceeds the threshold voltage the device is forced into conduction. Hence it results in the following term for the dv/dt capability:

$$\frac{dv}{dt} = \frac{V_{th}}{R_G \cdot C_{GD}} \quad (V_{GS} > V_{TH})$$

As you can see, low V_{th} devices are more prone to dv/dt turn-on. Because of the negative temperature coefficient of the threshold voltage, the dv/dt capability becomes worse at higher temperature and therefore also the gate impedance has to be chosen carefully to avoid this effect.

The second mechanism for a possible dv/dt turn-on is due to the parasitic BJT as shown in Figure 13. Between the base of the BJT and the drain of the MOSFET it appears as a C_{DB} donated capacitance, which associates with the depletion region of the body diode extending into the drift region. When there is a voltage range across drain and source, C_{DB} gives rise to current I_2 to flow through R_B .

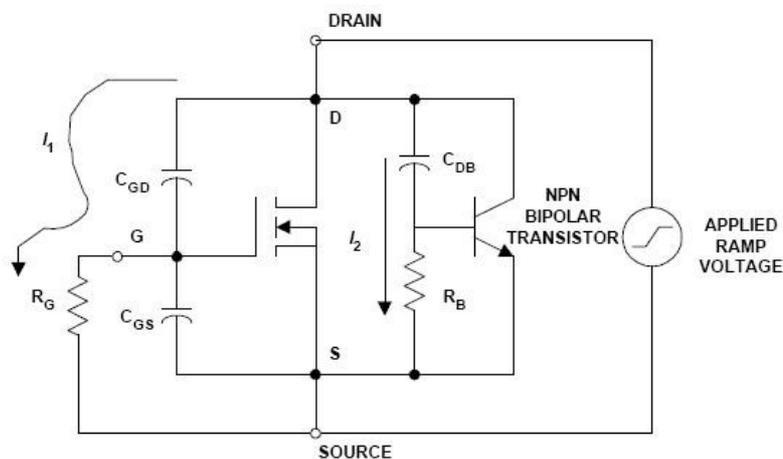


Figure 13: Two possible Mechanism for dv/dt capability turn-on

With analogy to the first mechanism the dv/dt capability here is:

$$\frac{dv}{dt} = \frac{V_{BE}}{R_B \cdot C_{DB}}$$

The parasitic BJT is turned on, if the voltage across R_B is greater than about 0,7V, because then the base-emitter junction is forward-biased. The breakdown voltage will be limited to the open-base breakdown voltage of the BJT for high dv/dt and large values of R_B . If now the applied drain voltage is higher than the open-base breakdown voltage the MOSFET enters avalanche and the destruction of the device is possible if the current is not limited externally. Increasing dv/dt capability requires the reducing of the base resistance R_B by increasing the body region doping and reducing the distance current I_2 . This current has to flow laterally before it is collected by the source metallization. BJT related dv/dt capability becomes worse at a higher temperature, because R_B increases and V_{BE} decreases with increasing temperature.

2.5 Dynamic Characteristics

In addition to the above mentioned static characteristics, each MOSFET also has specified dynamic characteristics, which are very important in circuit developing and can cause unintentional behavior or even damage to the device or/and the external circuit. The most important values for these characteristics are described in the datasheet of the MOSFET.

2.5.1 Transconductance

Under transconductance g_{fs} you appreciate the measure of the sensitivity of drain current to changes in the gate-source bias. It was commonly used in the field of electron tubes. This value is normally quoted for a special gate-source voltage that allows a drain current of about one half of the maximum current rating value and for a drain-source voltage that ensures operation in the constant current region. In other words, g_{fs} equals to the change in drain current divided by the change in the gate voltage for a constant drain voltage.

$$g_{fs}(\text{Siemens}) = \frac{dI_D(A)}{dV_{GS}(V)}$$

The transconductance is influenced by its gate width. It increases in proportion to the active area as cell density increases. The cell density of recent MOSFETs is about 8 million per square inch for planar MOSFETs and about 12 million per square inch for trench MOSFETs. Furthermore the transconductance is influenced by the channel width. A reduced channel length is favorably for the transconductance, but also for the on-resistance with punch-through as a tradeoff. This lower limit is today around 1 – 2 μm and is set by the ability to control the double-diffusion process. The last thing that affects the transconductance is the gate oxide thickness. The lower it is the higher the transconductance. It also varies with the operating conditions. The transconductance is zero, if the gate-source voltage is lower than the gate-threshold voltage, it is peaking at a finite value if the device is fully saturated or it is very small in the ohmic region, because the device cannot conduct more current.

2.5.2 Parasitic and Intrinsic Components

If the MOSFET is used in a dynamic operation mode, inside the MOSFET structure occur different parasitic components, which affect the dynamic behavior of the MOSFET. One of these components is a parasitic JFET between the two body implants. This JFET induces a restriction of current flow when the depletion widths of the two adjacent body diodes extend into the drift region with increasing drain voltage. This JFET is part of the normal operation and has significant influence on $R_{DS(on)}$.

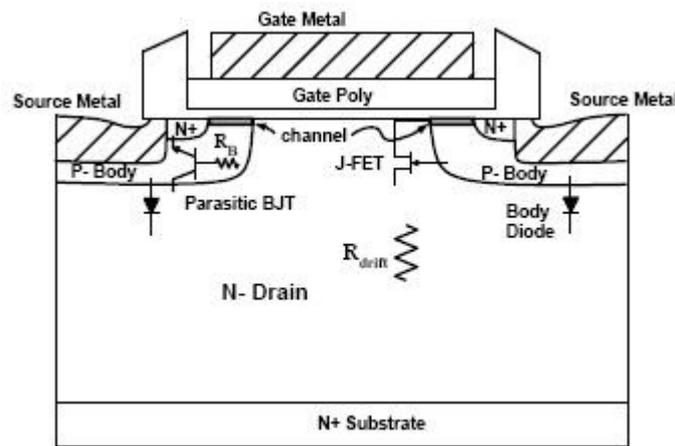


Figure 14: Power MOSFET cross-section with parasitic components

The body-drain PN junction forms an intrinsic diode called the body diode (see Figure 14). The body is shorted to the source so reverse drain current cannot be blocked, providing a high current path through the body diode. Enhancing the device and flowing reverse drain current reduces conduction loss, because electrons flow through the channel in addition to electrons and minority carriers flowing through the body diode. Because of its extensive junction area, the current ratings and thermal resistance of this diode exhibit a very long reverse recovery time and large reverse recovery current due to the long minority carrier lifetimes in the N⁻ drain layer. This eliminates the use of this diode except for very low frequency applications. In high frequency applications, the parasitic diode must be paralleled externally to ensure that the diode does not turn on, which would increase the device power dissipation due to the reverse recovery losses within the diode.

The third intrinsic component is a BJT, more precisely a NPN bipolar junction transistor, which is very susceptible to unwanted device turn-on and premature breakdown. If the BJT is turned on and saturated it would result in a so called latchup, where the MOSFET cannot be turned off again, except externally interrupting the drain current. There is high power dissipation during latchup which can destroy the device. To prevent this latchup, the base of the BJT is shorted to the source and if the base was allowed to flow the breakdown voltage would be greatly reduced. However theoretically this condition is still possible for extremely high dv/dt capability during turn-off, but it is very difficult to build a circuit capable which can achieve such high dv/dt . So there is still a risk of turning on the parasitic BJT if the body diode conducts and then commutates off with excessively high dv/dt . It can be build enough voltage across the body resistance to turn on the BJT, because high commutation dv/dt causes high current density of minority carriers in the body region. For this reason you have a peak commutating dv/dt limit in the datasheet of a MOSFET.

2.5.3 Intrinsic Capacitances

Beside the JFET, the BJT and the body diode there are also intrinsic capacitances whose values are determined by the structure of the MOSFET, the materials involved and the voltage across it. But in contrast to other MOSFET characteristics, the value of these intrinsic capacitances is independent on temperature, which is also a reason for the insensitive of the switching speed related to temperature. In a MOSFET the following capacitances can be found:

- **C_{iss} – Input Capacitance**

The input capacitance is measured between gate and source with the drain shorted to the source. You can describe it as the addition of the gate-source capacitance and the gate-drain capacitance ($C_{iss} = C_{GS} + C_{GD}$). The input capacitance must be charged to the threshold voltage before the device can

begin to turn on and similar discharge to the plateau voltage to turn the device off. Therefore C_{iss} and the impedance of the drive circuit have a direct effect on turn-on and turn-off delays.

- **C_{oss} – Output Capacitance**

The output capacitance is measured between the drain and the source with the gate shorted to the source. It is the addition of the gate-drain capacitance and the drain-source capacitance ($C_{oss} = C_{GD} + C_{DS}$). This capacitance is very important by soft switching applications, because it can affect the resonance of the circuit.

- **C_{rss} – Reverse Transfer Capacitance**

The reverse transfer capacitance is measured between drain and gate with the source connected to ground. It is another indication for the gate-drain capacitance C_{GD} which is also often referred to as Miller Capacitance. This capacitance is one of the major parameters affecting voltage rise and fall times during switching. It also effects turn-off delay times.

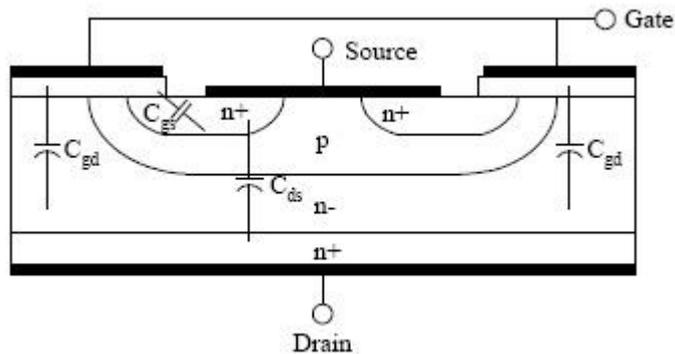


Figure 15: Power MOSFET Structure Capacitances

These names for the three capacitances you can find in the datasheet of the MOSFET, but there are also names which are closer to the physical meaning of them. Some of them are already mentioned above:

- **C_{GS} – Gate-Source Capacitance**

The gate-source capacitance is a parallel connection of C_{oxN+}, C_{oxP} and C_{oxm}. As the N+ and P regions of a Power MOSFET are highly doped, C_{oxN+} and C_{oxP} can be considered as constant. C_{oxm} is the capacitance between the gate and the source electrode, so between a polysilicon and a metal electrode and thus it is also constant. Therefore you can consider that the gate-source capacitance is a constant capacitance, whose value does not depend on the transistor state and the applied voltage.

- **C_{GD} – Gate-Drain Capacitance**

The gate-drain capacitance can be seen as the series connection of two elementary capacitances, C_{oxD} and C_{GDj}. C_{oxD} is the oxide capacitance constituted by the gate electrode, the silicon dioxide and the top of the N epitaxial layer. This is a constant value. C_{GDj} in contrast is caused by the extension of the space-charge zone when the MOSFET is off-state. Therefore it is dependent upon the drain-source voltage and thus a non-linear function of voltage. From this you can calculate the value of C_{GD} like this:

$$C_{GD} = \frac{C_{oxD} \cdot C_{GDj}(V_{GD})}{C_{oxD} + C_{GDj}(V_{GD})}$$

The value of C_{GDj} can be approximated using the expression of the plane capacitor:

$$C_{GDj} = A_{GD} \cdot \frac{\epsilon_{Si}}{\omega_{GDj}}$$

Where A_{GD} is the surface area of the gate-drain overlap, ε_{Si} is the permittivity of the silicon and ω_{GDj} is the width of the space-charge region and is given by:

$$\omega_{GDj} = \sqrt{\frac{2 \cdot \epsilon_{Si} \cdot V_{GD}}{q \cdot N}}$$

Where q is the electron charge and N is the doping level. Therefore it is:

$$C_{GDj}(V_{GD}) = A_{GD} \cdot \sqrt{\frac{q \cdot \epsilon_{Si} \cdot N}{2 \cdot V_{GD}}}$$

From this equation it can be seen that the value of C_{GDj} (and thus of C_{GD}) is dependent upon the gate-drain voltage. If this voltage increases the capacitance decreases. Is the MOSFET in on-state mode, C_{GDj} is shunted and the C_{GD} remains equal to C_{oxD} and thus a constant value.

- **C_{DS} – Drain-Source Capacitance**

As the source metallization overlaps the P-wells the drain and source terminals are separated by a PN junction. Therefore C_{DS} is the junction capacitance which is also non-linear and its value can be calculated using the same equation as for C_{GDj} . It varies inversely with the square root of the drain-source bias.

2.5.4 Gate Charge

The charge on the gate terminal is meant with gate charge which is determined by the gate-source capacitance. The lower the gate charge, the easier driving the MOSFET. The total gate charge Q_G affects the highest reliable switching frequency in fact the lower the total gate charge, the higher the frequency. With a higher gate charge lower values and smaller sizes for capacitances and inductors in the drive circuit are required which are significant factors in system costs.

The main advantage of the gate charge is the possibility of easy calculation of gate current to turn on the MOSFET for comparing the switching performance of two or more devices from different manufactures. Capacitances do not tend themselves to calculation of gate current required to switch device in a given time. It does not provide accurate results by comparing switching performance of two devices. The calculation with total gate charge on the contrary just results in the multiplication of current and time. At a total gate charge of 20nC the device can be turned in 20ms if the drain current is 1mA or turned on in 20ns if the drain current is 1A.

The gate charge is inter-related to the on-state resistance, the lower the gate charge, the higher the on-state resistance and vice versa. So there is a trade-off between the on-state resistance and the gate charge and the application has to decide which parameter is more important. With the multiplication of on-resistance and total gate charge you get the figure of merit (FOM) which can be used to compare different power MOSFETs for use in high frequency applications.

2.5.5 Switching Operation

As described earlier in this paper, power MOSFETs can switch at very high speed, because of their unipolar nature and there is no need to remove minority carriers as with bipolar devices. The only intrinsic limitation in communication speed is due to the internal capacitances of the MOSFET. These capacitances must be charged or discharged when the transistor switches and this can be a relatively slow process. Furthermore the driver circuit is responsible for the communication speed, because it limits the current which flows through the gate capacitance.

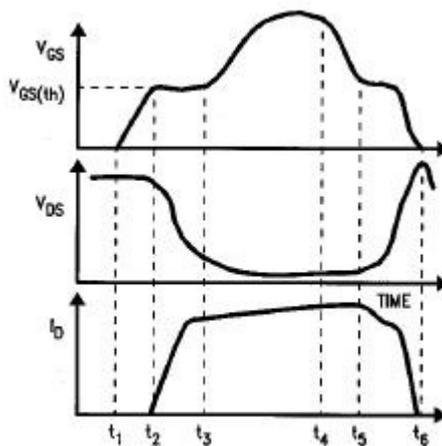


Figure 16: Switching Waveforms for Resistive Load

There are several different phenomena occurring during turn-on. In the time interval between t_1 and t_2 the initial turn-on delay time $t_{d(on)}$ can be seen which is dependent from the length of time it takes gate-source voltage to rise to the

threshold voltage $V_{GS(th)}$. The time constant can be calculated as the multiplication of R_S and C_{GS} . The typical time-on delay time approximation is:

$$t_{d(on)} = R_S \cdot C_S \cdot 1n \cdot \left(1 - \frac{V_{GS(th)}}{V_{DS}} \right)$$

In the time interval t_2 and t_3 , the gate-source voltage has reached the threshold voltage value and the MOSFET begins to draw increasing load current and the drain-source voltage decreases. On the one hand the gate-drain capacitance has to discharge, but on the other hand its value also increases since it is inversely proportional to the drain-source voltage:

$$C_{GD} = \frac{C_{GD}(0)}{V_{GD}}$$

Unless the required current to discharge C_{GD} cannot be quickly supplied by the gate driver, the voltage fall will be slowed with increasing in turn-on time.

In the time interval between t_3 and t_4 the MOSFET is on so that the gate voltage can rise to the overdrive level.

The last interval between t_4 and t_6 is the turn-off interval in which the turn-off occurs in reverse order. The gate-source voltage must drop back to the threshold voltage value before the on-state resistance will start to increase. As the drain-source voltage starts to rise, the Miller effect due to gate-drain capacitance re-occurs and impedes the rise of the drain-source voltage as the gate-drain capacitance recharges to V_{CC} .

2.6 Temperature Effects

The temperature can affect the behavior and characteristics of the power MOSFET, so it is reasonable to take a lot at the possible consequence of temperature.

2.6.1 Switching Speed

Both the switching speed and the switching loss are practically unaffected by temperature, because the capacitances are unaffected by temperature (see Switching Operations). However the reverse recovery current of the body diode in the MOSFET increases with temperature and so this diode affects turn-on switching loss.

2.6.2 Threshold Voltage

The threshold voltage can be seen mostly as turn-on specification. It tells how many milliamps of drain current will flow at $V_{GD(th)}$, so that the device is basically off, but on the verge of turning on. The threshold voltage has a negative temperature coefficient, which means it decreases with increasing temperature. This behavior affects turn-on and turn-off delay times.

2.6.3 Transfer Characteristics

The transfer characteristic depends on temperature as well as on drain current. In figure 15 you can see that below 4 Amps the gate-source voltage has a negative temperature coefficient and above 4 Amps the temperature coefficient is positive.

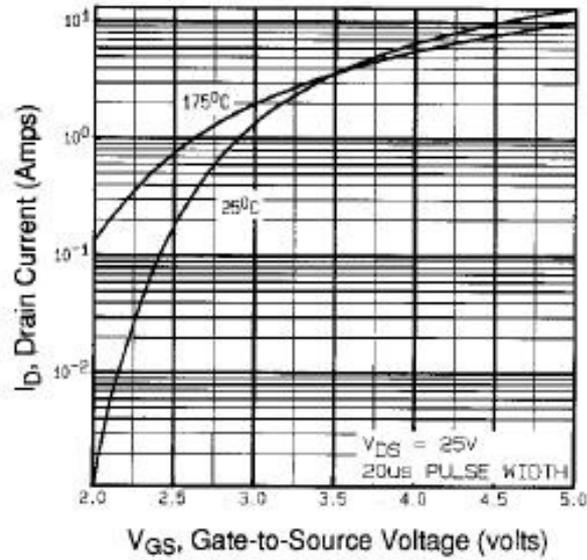


Figure 17: Transfer Characteristics

2.6.4 Breakdown Voltage

As described in the topic static electrical characteristics, the breakdown voltage has a positive temperature coefficient and thus it is dependent on temperature.

2.7 Thermal and Mechanical Characteristics

- **$R_{\theta JC}$ – Junction to Case Thermal Resistance**

This is the thermal resistance of the junction of the die to the outside of the device case. In general, heat is the result of power lost in the device itself and the thermal resistance relates how hot the die gets relative to the case based on the power loss.

- **$Z_{\theta JC}$ – Junction to Case Transient Thermal Impedance**

The junction to case transient thermal impedance takes into account the heat capacity of the device. It is used to estimate instantaneous temperatures resulting from the power loss on transient basis. You can build a transient thermal impedance RC model for measurement of single pulse transient thermal impedance response (see Figure 18).

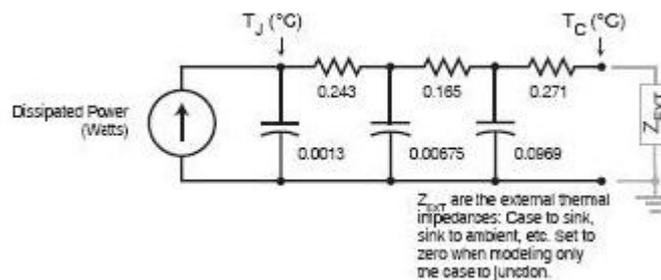


Figure 18: Transient Thermal Impedance RC Model

For simulating temperature rise with this model you have to apply a current source whose magnitude is the power being dissipated in the MOSFET. You can estimate the junction to case temperature rise as the voltage across the ladder by setting Z_{EXT} to zero (a short).

In the datasheet of the MOSFET is a transient thermal impedance “family of curves”, which is a rectangle pulse simulation based on the RC thermal impedance model and shows the maximum effective transient thermal impedance, junction to case. With this curves you are able to estimate peak temperature rise for rectangle power pulses, which is common in a power supply, for example. However this graph is only relevant for switching frequencies less than 100 kHz, because the minimum pulse width is 10 μ s. At higher frequencies you can simply use the thermal resistance $R_{\theta JC}$.

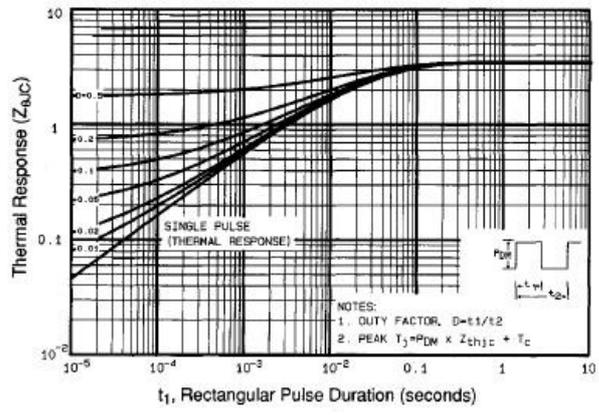


Figure 19: Thermal Impedance "Family of Curves"

2.7.1 Thermal Model

MOSFETs operate at elevated junction temperature and it is therefore important to observing their thermal limitations to achieve acceptable performance and reliability. In the datasheet of the MOSFET are a lot of information, for example the maximum junction temperature T_{Jmax} , the safe operating area or electrical characteristics as a function of T_J .

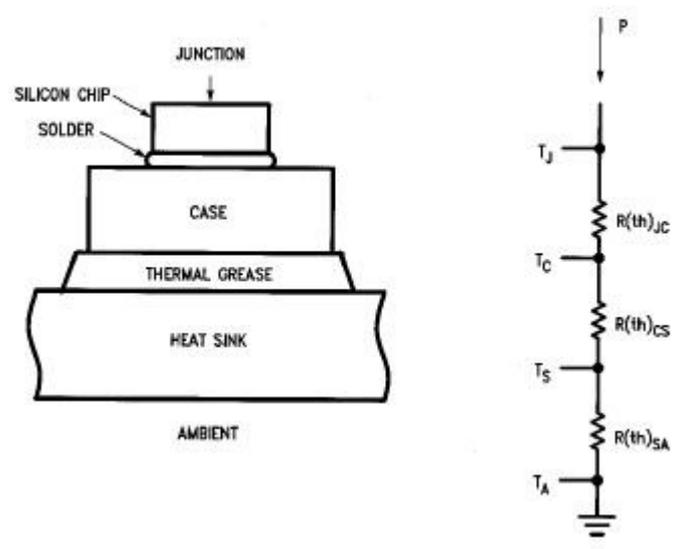


Figure 20: MOSFET Steady-State Thermal Resistance Model

You can see the elementary, steady-state thermal resistance model for the MOSFET and the electrical analogue in Figure 20. The heat, which is generated at the junction, flows through the silicon pellet to the case and then to the heat sink, if used. The junction temperature rise above the surrounding environmental is directly proportional to this heat flow and the junction to ambient thermal resistance. The steady-state thermal resistance $R_{\theta JA}$ between device junction and ambient is given as:

$$R_{\theta JA} = \frac{T_J - T_A}{P} \left(\frac{^{\circ}C}{W} \right)$$

Where:

T_J : average temperature at device junction ($^{\circ}C$)

T_A : average temperature at ambient ($^{\circ}C$)

P : average heat flow in watts (W)

As you can see, two different temperature reference points must be specified to get meaningful information about the thermal resistance. You can find the location of these points symbolically in the model for the junction temperature (T_J), the case temperature (T_C), the sink temperature (T_S) and the ambient temperature (T_A). With these temperature references the following thermal resistances are defined:

$R_{\theta JC}$: Junction to Case Thermal Resistance

$R_{\theta CS}$: Case to Sink Thermal Resistance

$R_{\theta SA}$: Sink to Ambient Thermal Resistance

As shown in Figure 20, the junction to ambient thermal resistance is the series connection of all three individual resistances and thus:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA}$$

The junction to case thermal resistance is determined by the design and the manufacture and thus it can vary from device to device.

The power dissipation by the MOSFET depends upon the junction temperature T_J . From the both equations above for $R_{\Theta JA}$ you can set up an equation for it:

$$T_J = T_A + P \cdot (R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA})$$

To find a maximum for $R_{\Theta SA}$, to ensure stability, you must either use an iterative or graphical solution. However the steady-state thermal resistance is not satisfactory for finding peak junction temperatures for pulsed applications. Solving this problem means using the transient thermal resistance model.

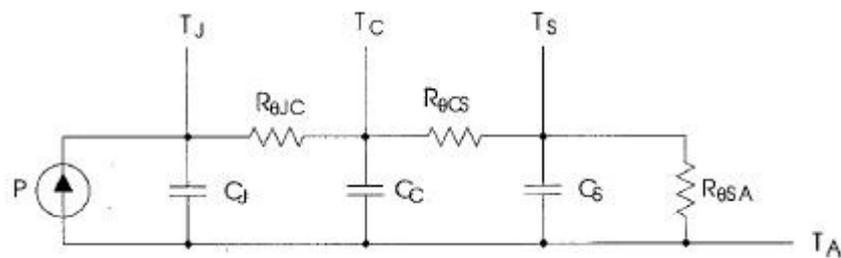


Figure 21: Transient Thermal Resistance Model

At the end of a power pulse, a peak power value results in overestimating the actual junction temperature while an average power value underestimate the peak junction temperature. The reason for this purpose lies in the thermal capacity of the MOSFET and its housing, for example its ability to store heat and to cool down before the next pulse. If you assume that current is evenly distributed across the silicon chip in the MOSFET and that the only significant power losses occur in the junction, then you can use the simplified model in Figure 21, in which the thermal capacitances are lumped into single capacitors labeled C_J , C_C and C_S . When there is a step pulse of heating power at the junction, the junction temperature will rise exponentially to some steady-state value, like it is shown in Figure 22. This value depends on the response of the thermal network. Once the power input is terminated at t_2 , the junction temperature will decrease again along the curve indicated by T_{cool} in Figure 22 back to its initial value.

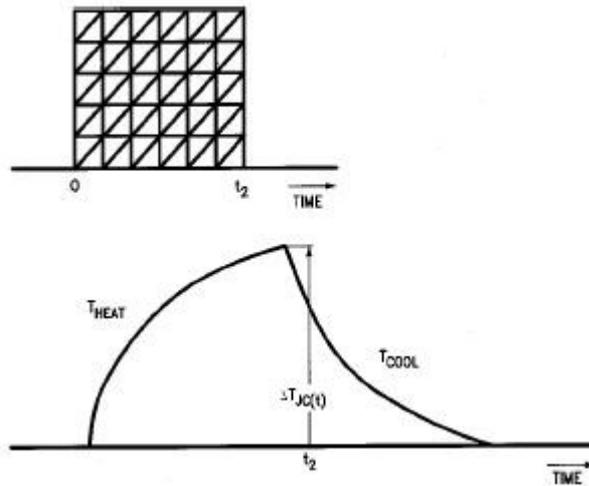


Figure 22: Junction Temperature Response to a Step Pulse of Heating Power

From this curve you can determine the transient thermal resistance:

$$Z_{\theta JC} = \frac{\Delta T_{JC}(t)}{P}$$

The transient thermal resistance curve approaches the steady-state value at long times and the slope of the curve for short times is inversely proportional to C_J .

For a series of power pulses, superposition of these pulses offers a rigorous numerical method of using the transient thermal resistance curve, to secure a good solution for T_J . With this method you can test the response of a network to any input function. To do this, you have to replace the input function by an equivalent series of superimposed negative and positive step functions. Each of these step functions must start at zero and continue to the time which T_J is computed for. Figure 23 shows a typical example for the train of heating pulses.

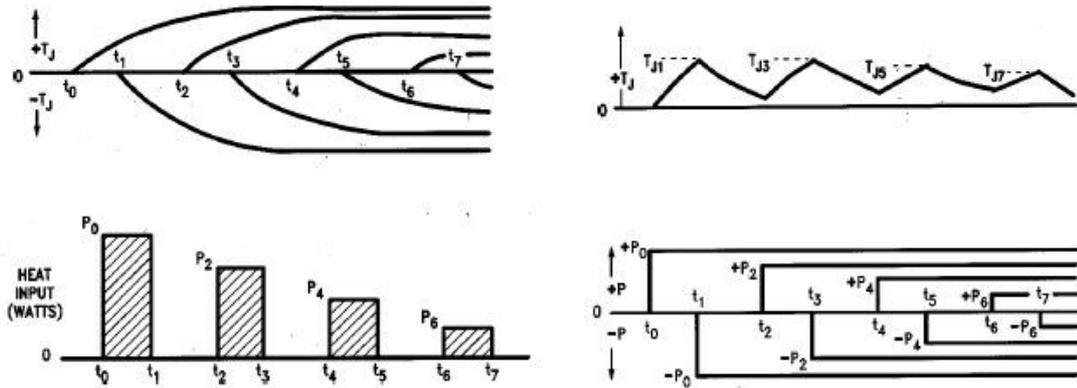


Figure 23: top left – Heat Input; top right – Equivalent Heat Input by Superposition of Power Pulses; bottom left – Junction Temperature Response to Individual Power Pulse; bottom right – Use of Superposition to Determine Peak T_J

T_J at time is given by:

$$T_J(t) = T_J(0) + \sum P_i \cdot [Z_{\Theta JC}(t_n - t_i) - Z_{\Theta JC}(t_n - t_i + 1)]$$

To compute the peak junction temperature at thermal equilibrium for a train of equal amplitude power pulses, as shown in Figure 24, you first have to plot the bracketed expression to simplify the further calculation. This plot is shown in Figure 19 and presents the thermal impedance “family of curves”.

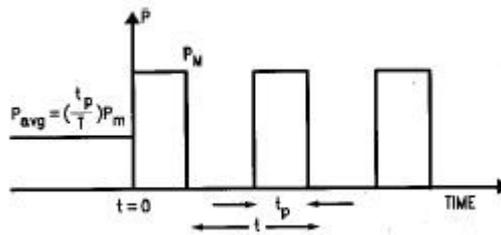


Figure 24: Train of Power Pulses

From the curve in Figure 19, you can readily calculate T_J if you know P_M , $Z_{\Theta JC}$ and T_C using the expression:

$$T_J = T_C + P_M \cdot Z_{\Theta JC}$$

3 Project Simulation

Before starting with applied measurements in a project, it is expedient and recommended to simulate the intended circuit virtual on computer. With such a simulation you easily get a fast overview of the circuit behavior and are able to make changes in the set-up very quick. The software Micro-Cap 9 by Spectrum Software is used here.

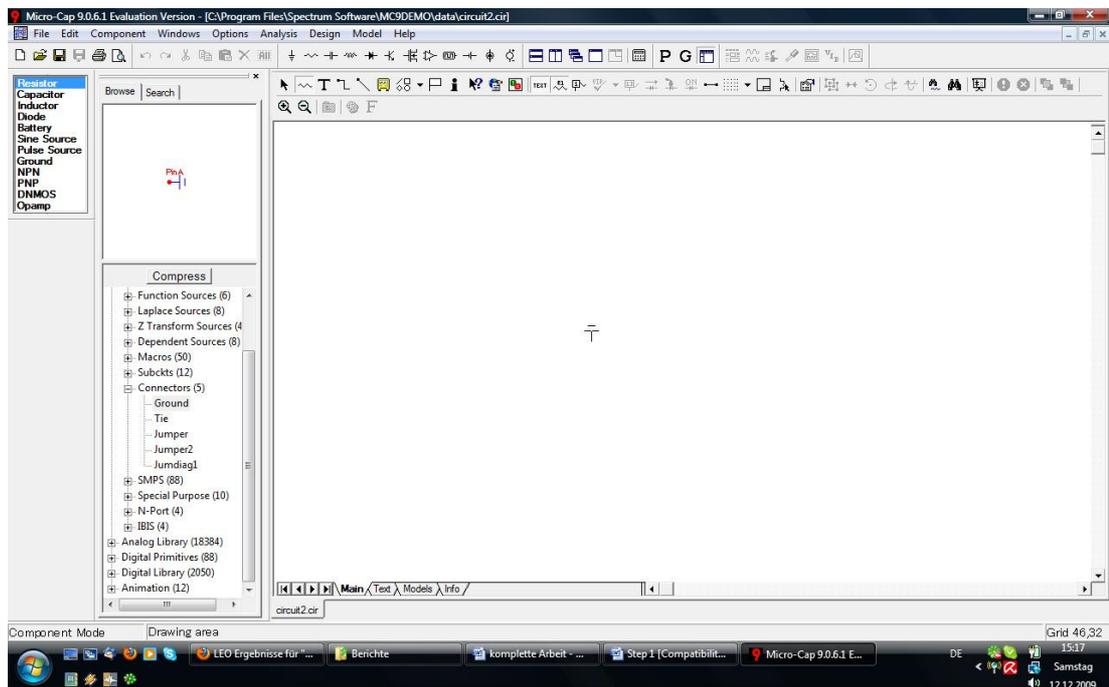


Figure 25: Screen Shot of Micro-Cap 9

3.1 Heating a MOSFET Power Transistor

The first and in this case also the only one is the simulation of a circuit, whose only function is heating the Power MOSFET to and above its published operating ranges for temperatures. This circuit should be as easy as possible. Therefore it only consists of three parts: a power supply for the gate-source voltage, a power supply for the drain-source voltage and the power MOSFET itself. Like mentioned in the

introduction, for all experiments and thus of course for the simulations, too, an IRLZ14 Power MOSFET is used. You can find its datasheet with all important values in the appendix.

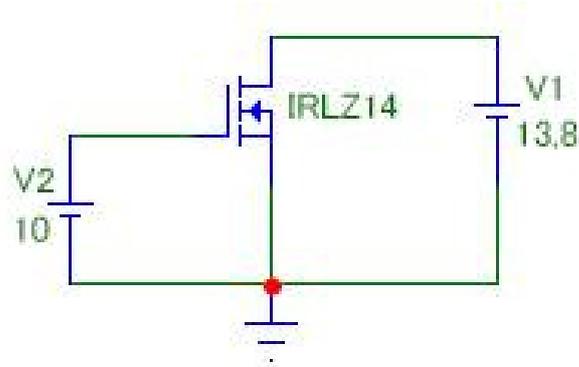


Figure 26: Circuit for Heating the Power MOSFET

With the simulation of the circuit shown in Figure 26 you get two different, for this project required charts. The first one shows the current I_D against the voltage of V1 for different gate-source voltages and the second one shows the power P_{MOS} against the voltage of V1 for different gate-source voltages.

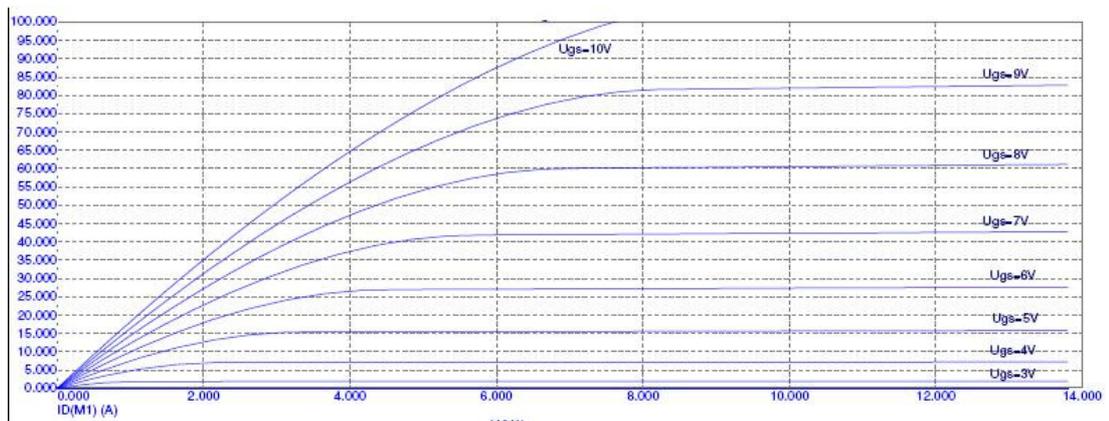


Figure 27: I_D against $V(V1)$ for different gate-source voltages

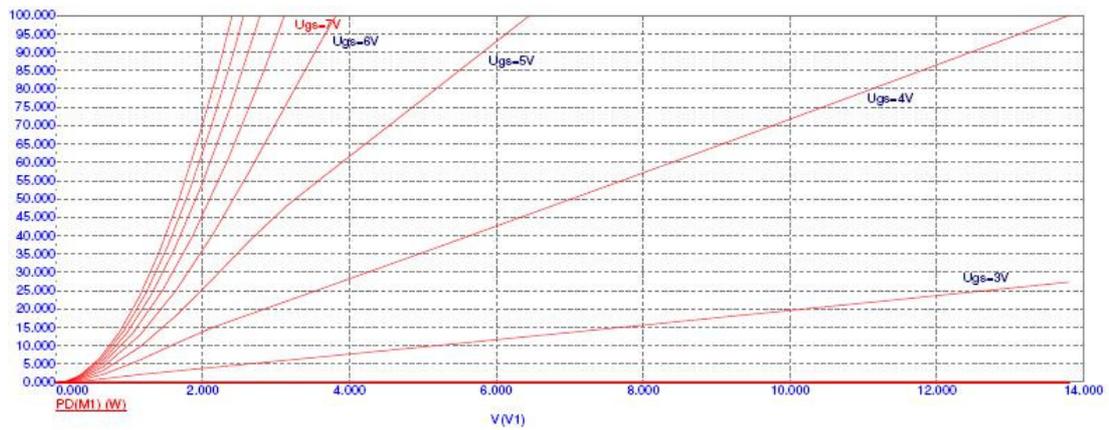


Figure 28: PD(MOSFET) against V(V1) for different gate-source voltages

From these two charts you can directly see that not much drain-source voltage and according to this not much drain current is necessary to heat up the MOSFET, because in this circuit no resistance for current limiting is used. You have to work with low voltages and current otherwise the MOSFET will be destroyed very fast. To figure out which adjustments are the best for the volitional result, test measurements are essential. The right adjustments are up to the desired steady-state temperature the MOSFET should achieve.

4 Project Measurements

The goal of the measurements in this project is collecting data to get information about the heat transfer characteristics of the power MOSFET. For this reason a multitude of measurements have to be made with different MOSFET mountings and different distances of the Thermocouples to the case of the MOSFET. The first measurements had been made without an enclosure with an upright and a side mounted power MOSFET. No enclosure means here, that no direct enclosure was used, just a bigger cardboard to cover any external influences like wind. For the second series of measurements an aluminum enclosure was used to detect a theoretical influence of the enclosure.

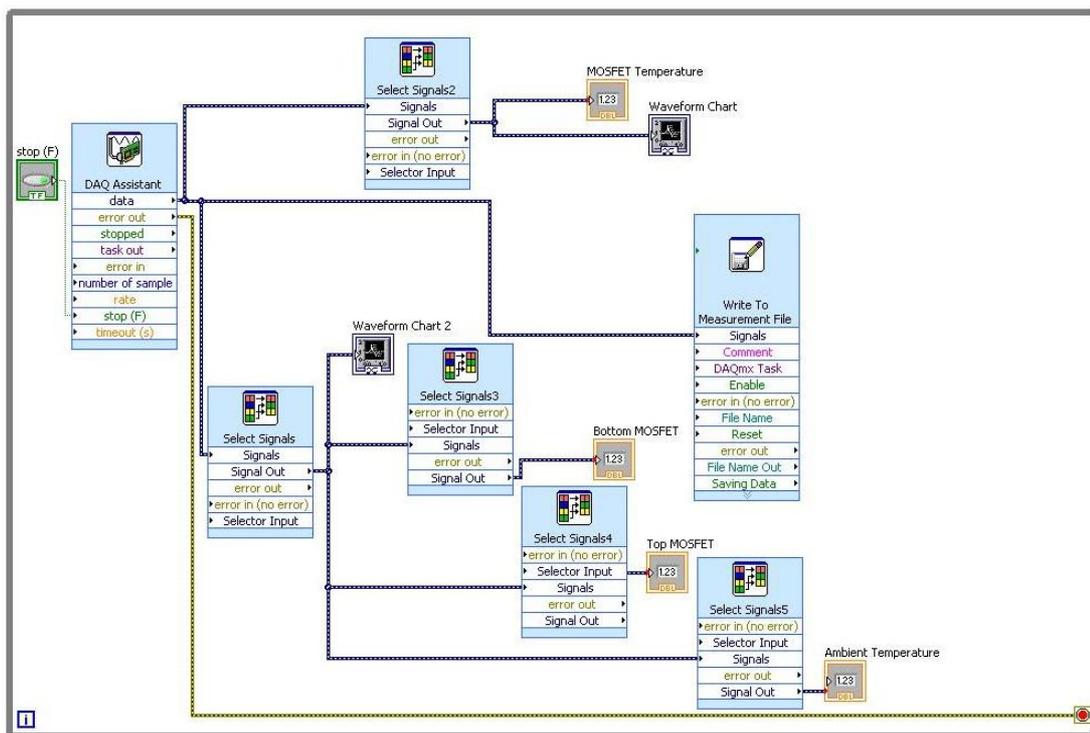


Figure 29: LabVIEW Block Diagram for temperature measurements

As Hardware for the measurements a CompactDAQ Chassis NI cDAQ-9172, a 4-Channel Thermocouple Input Module NI 9211 (in slot 5 of the chassis) by National Instruments and Omega Precision Fine Wire Thermocouples 5TC-GG-K-24-72 were used. As software to control the components and show the results on the screen LabVIEW had been used. The block diagram is shown in Figure 29. On the one hand,

the collected data is shown in two different graphs in the front panel (Figure 30) and on the other hand the data is stored in a file on the PC. For a better readability and monitoring digital indications show the current temperature values.

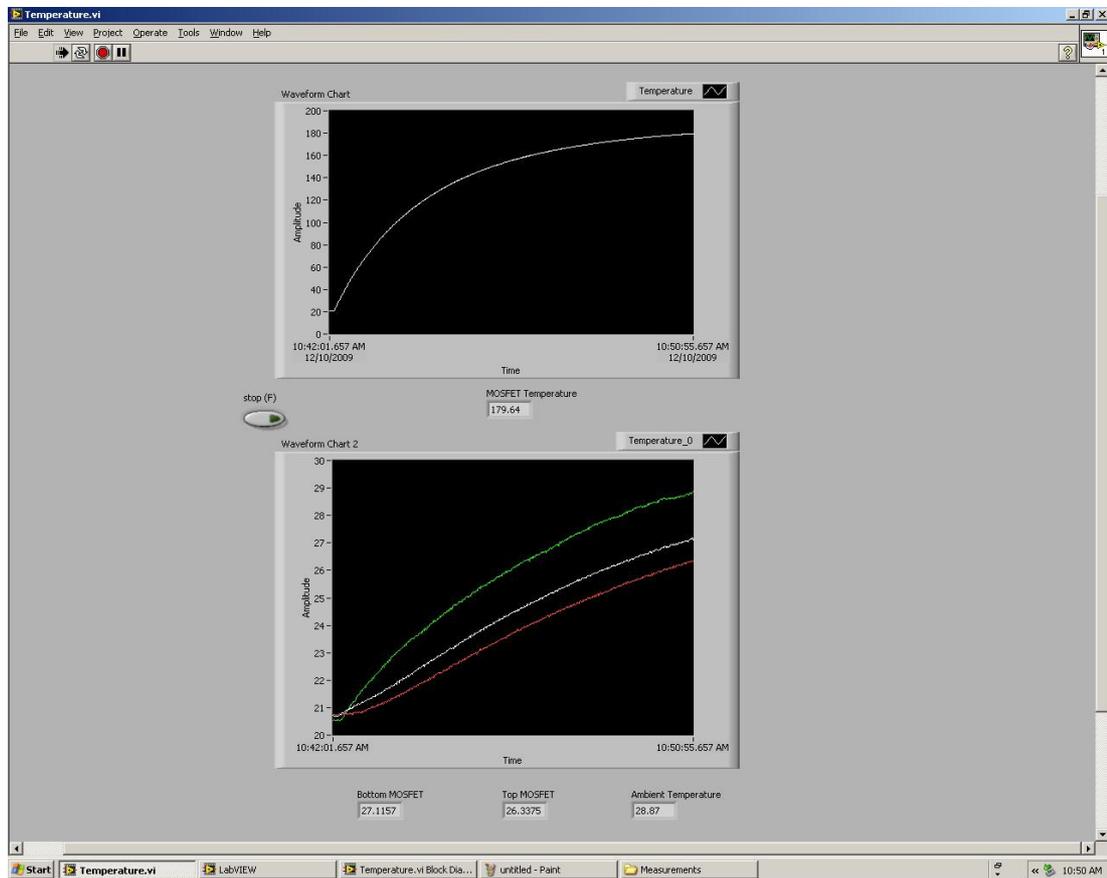


Figure 30: LabVIEW Front Panel for temperature measurements

In each measurement four different values are detected via four thermocouples. The positions of two of these thermocouples vary for each mounting. While the mounting for the case temperature thermocouple and the ambient temperature thermocouples is the same in each mounting, the position of the other two thermocouples changes from side and front thermocouple in the upright mounting, to bottom and top thermocouple in the side mounting.

4.1 Measurements without Enclosure

In this series of measurements the test set-up had been secured from external influences by a cardboard. Inside this cardboard, on the top, the thermocouple for the ambient temperature is fixed. This series is divided into two parts, addicted to the mounting of the MOSFET. First the upright mounting and second the side mounting.

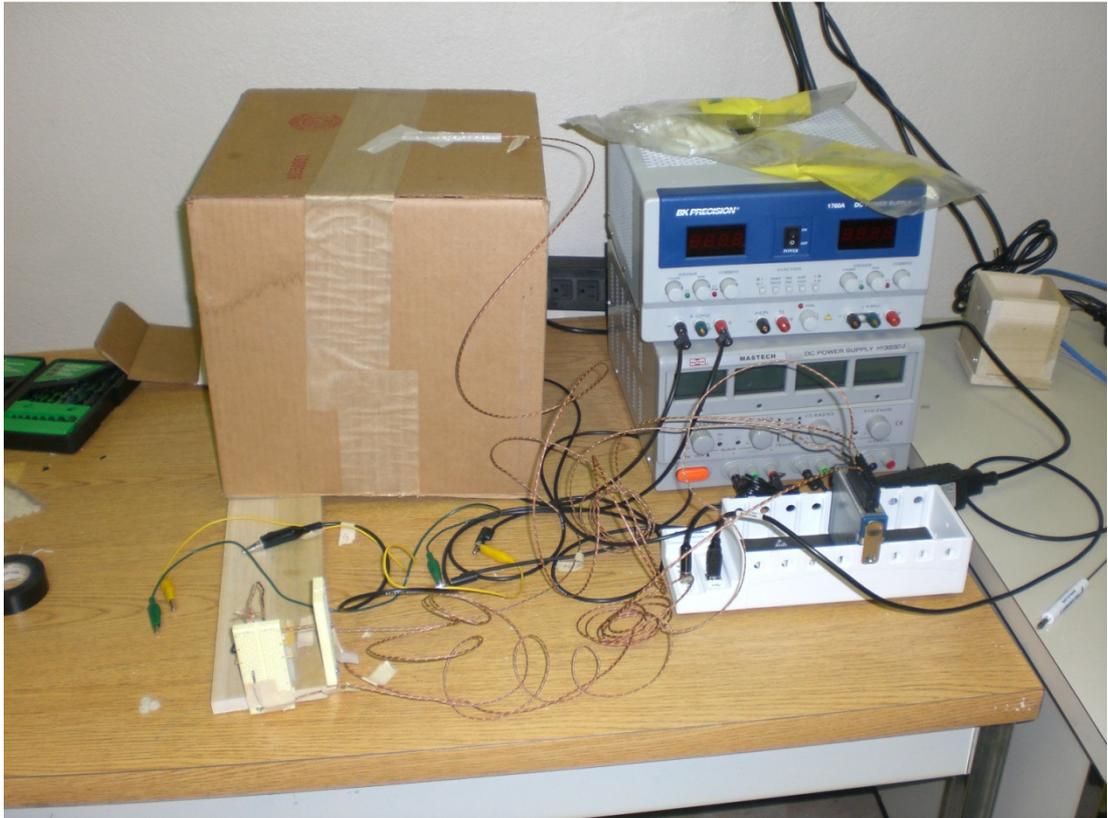


Figure 31: Experimental Set-up for measurements without enclosure

4.1.1 Upright Mounting

The Power MOSFET is mounted vertically on the PCB. The PCB itself was fixed with four spacers on a wooden mounting plate. To measure the temperatures around the MOSFET, the thermocouples were placed in front and beside the MOSFET, both in a height of 20mm from the PCB, but in every measurement in a different distance from the MOSFET (1mm, 2mm, 4mm, 6mm, 8mm, 10mm). The thermocouple for the ambient temperature was fixed on the top of the cardboard in a height of 24.82cm from the MOSFET during the measurements. For all measurements the following adjustments were used:

$$V_{GS} = 4V$$

$$I_D = 5.5A$$

$$V_{DS} = 0.8V$$

Each of the six measurements took about 15 minutes until the temperature values obtain a steady state value.

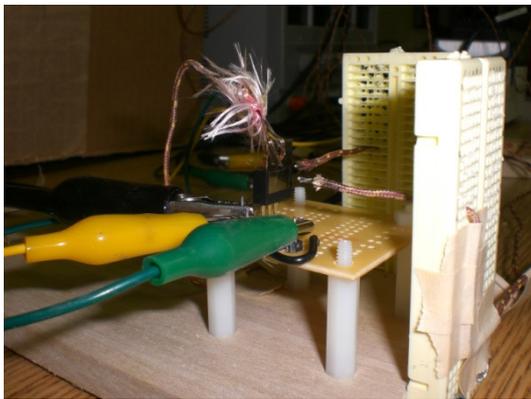


Figure 32: Set-Up Upright Mounting Side View

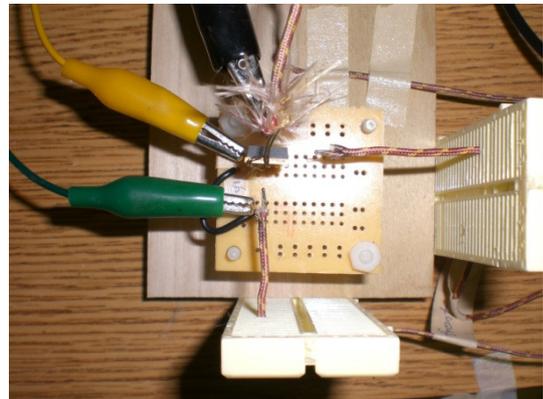


Figure 33: Set-Up Upright Mounting Top View

The steady state case temperature of the MOSFET with these adjustments was about 187°C.

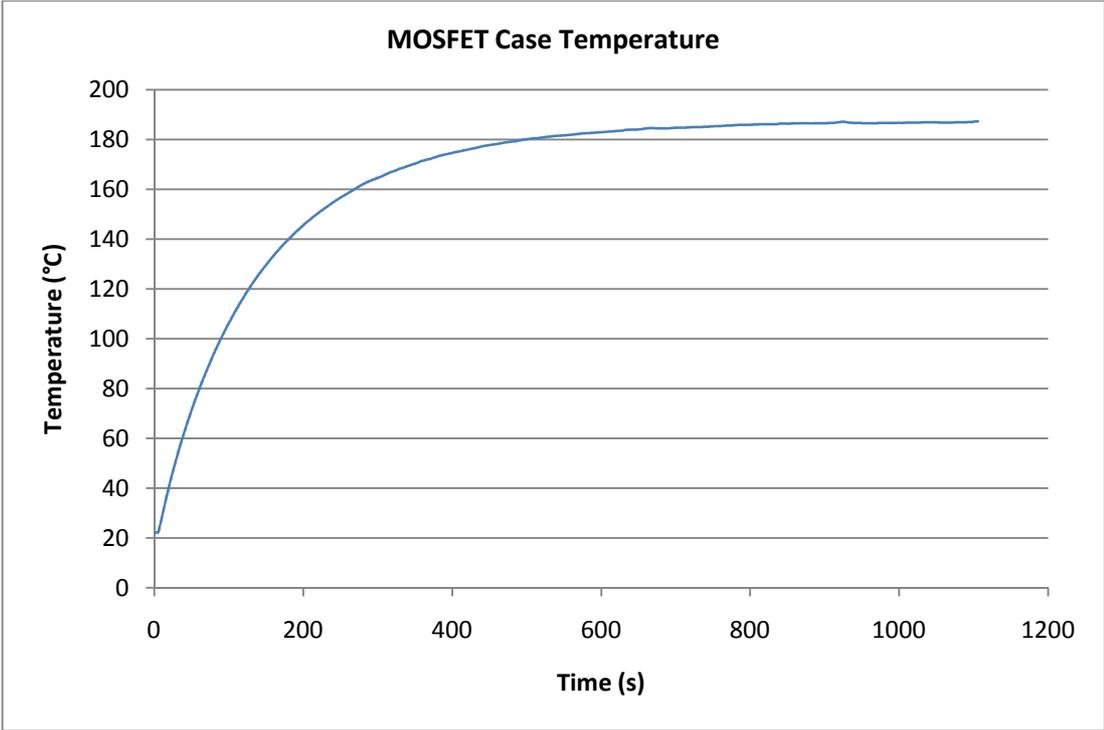


Figure 34: MOSFET Case Temperature (Upright Mounting)

This graph is almost the same for each measurement, the graphs for the other thermocouples vary for each distance, of course. Thus, you get six different graphs:

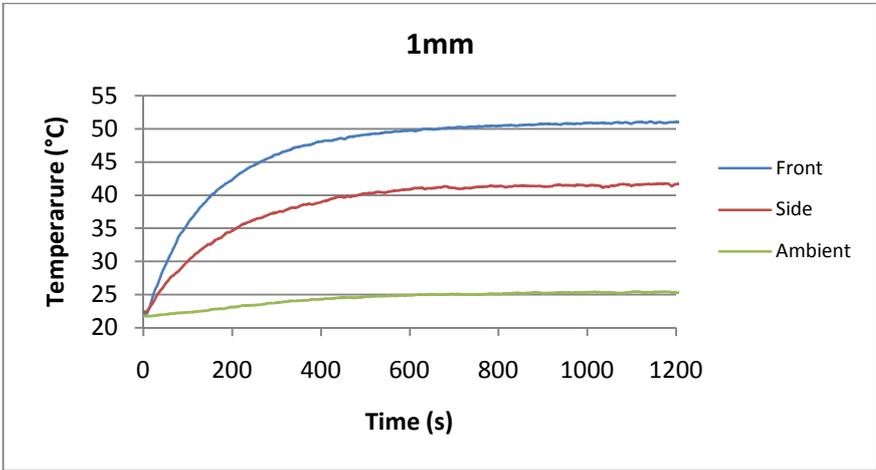


Figure 35: Surrounding Temperature Effects 1mm Distance (Upright Mounting)

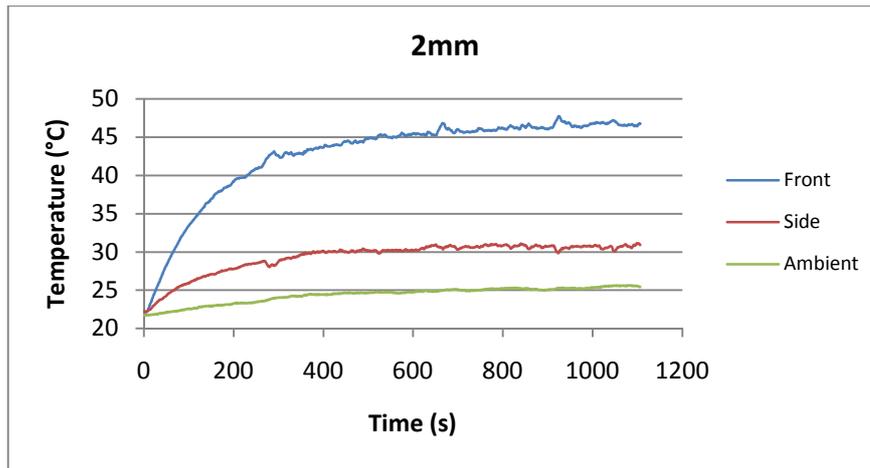


Figure 36: Surrounding Temperature Effects 2mm Distance (Upright Mounting)

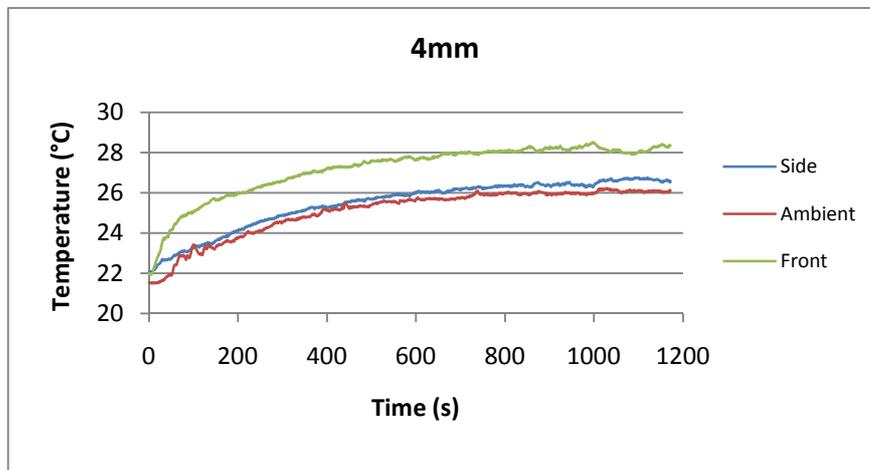


Figure 37: Surrounding Temperature Effects 4mm Distance (Upright Mounting)

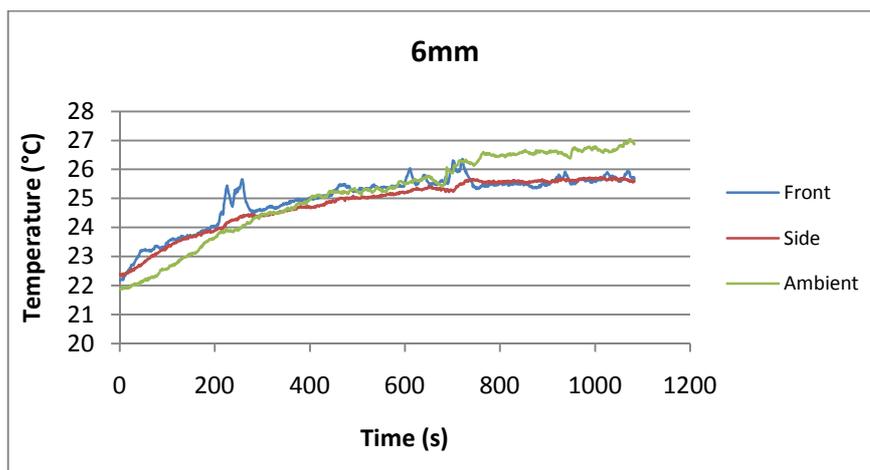


Figure 38: surrounding Temperature Effects 6mm Distance (Upright Mounting)

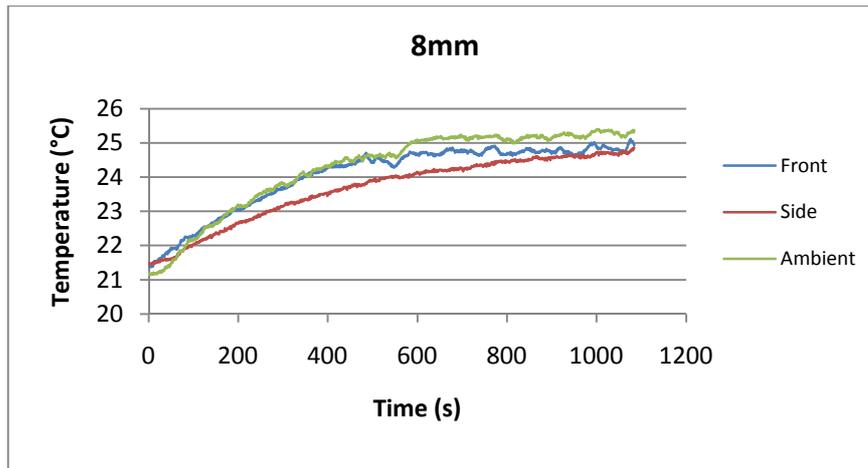


Figure 39: Surrounding Temperature Effects 8mm Distance (Upright Mounting)

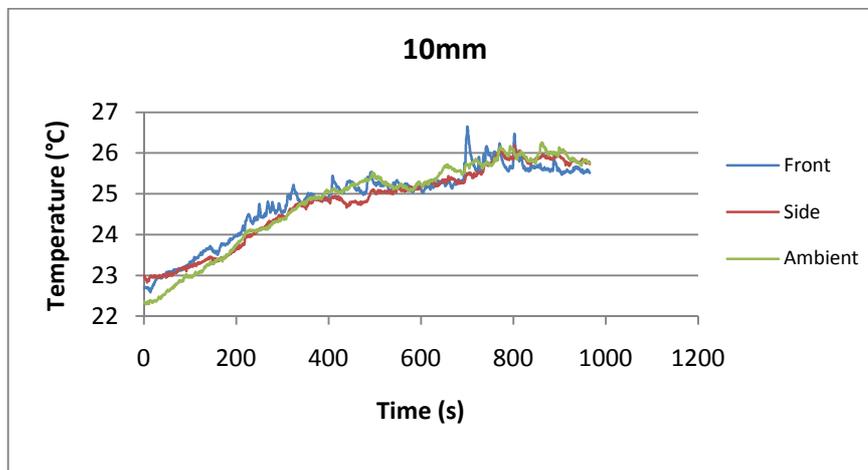


Figure 40: Surrounding Temperature Effects 10mm Distance (Upright Mounting)

Of these six graphs for the front and the side temperatures you can build one graph for each effect. So you have a better overview of temperature differences for each distance from the MOSFET. The first demonstrative attribute is the higher temperature in front of the MOSFET compared to the side temperature. The reason for this is be the bigger front area of the MOSFET compared to the side area. Furthermore the fast decrease of the temperature according to the increasing of the distance is very noticeable. At a distance of 4mm the side temperature has already reached the value of the ambient temperature, whereas the front temperature is still a little bit higher. At a distance of 6mm the front, side and ambient temperature are almost equal.

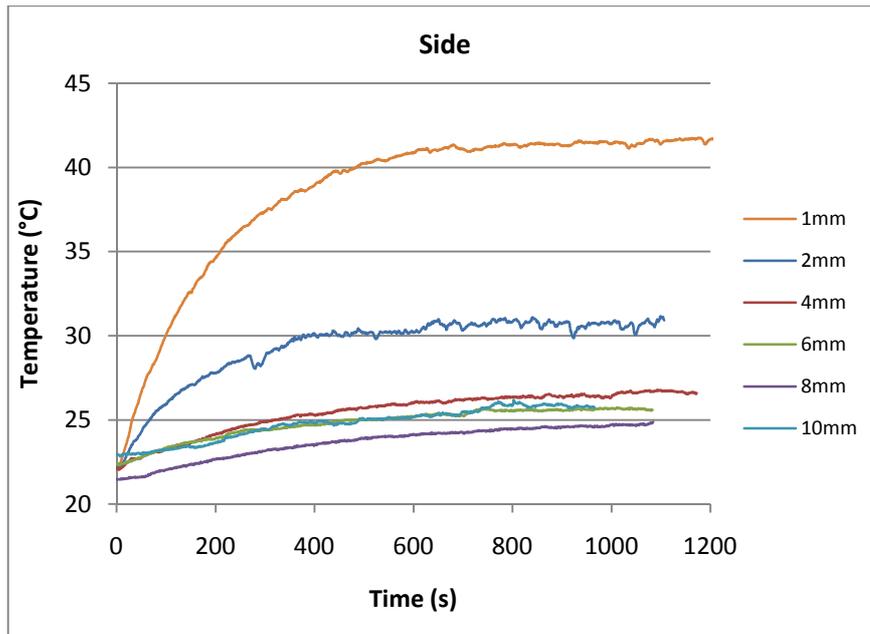


Figure 41: Surrounding Temperature Effects beside the MOSFET (Upright Mounting)

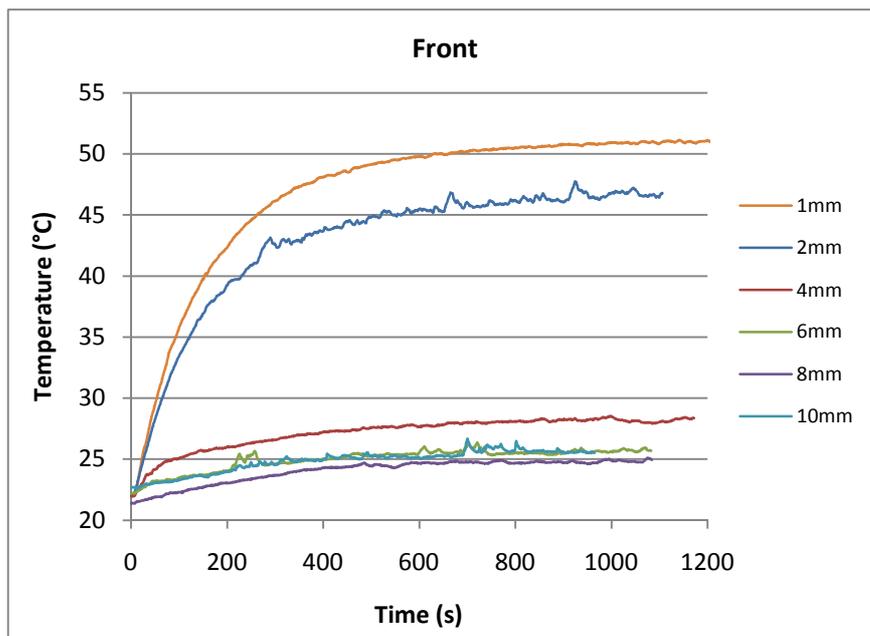


Figure 42: Surrounding Temperature Effects in the Front of the MOSFET (Upright Mounting)

To clarify the differences in temperature between front and side a new graph shows the connection of temperature of the distance (Figure 43). You can also see that the front and the side temperature is nearly the same from 6mm distance, like mentioned before.

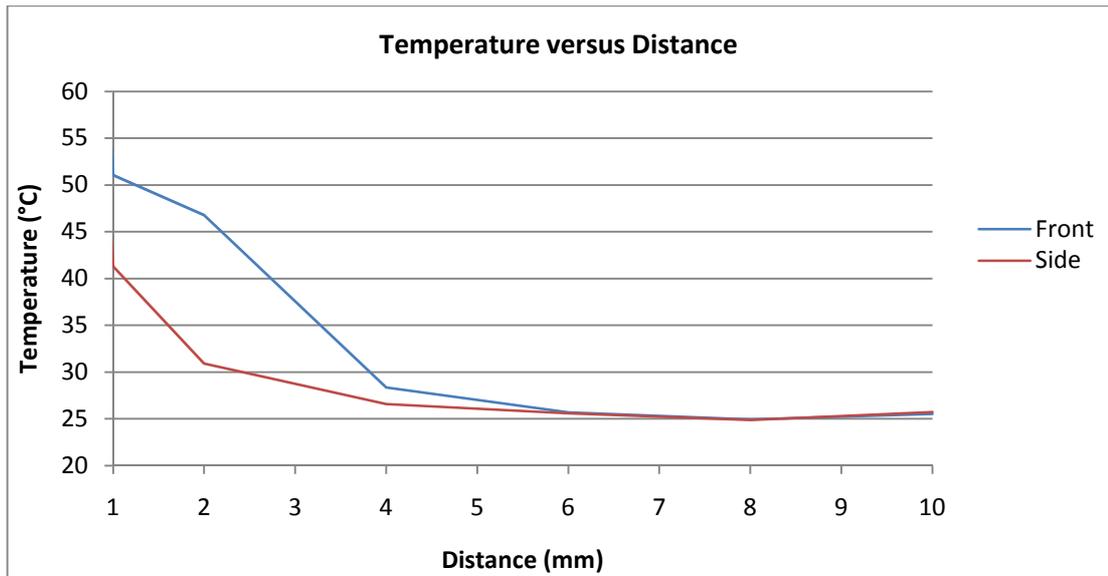


Figure 43: Comparison Temperature versus Distance after 1000sec (Upright Mounting)

4.1.2 Side Mounting

For the second series of measurements the mounting of the MOSFET was changed to discover, if the mounting of the MOSFET has any influence on the surrounding temperature effects. Therefore the PCB with the MOSFET was now fixed on the wooden side plate, so that the MOSFET now lied horizontally.

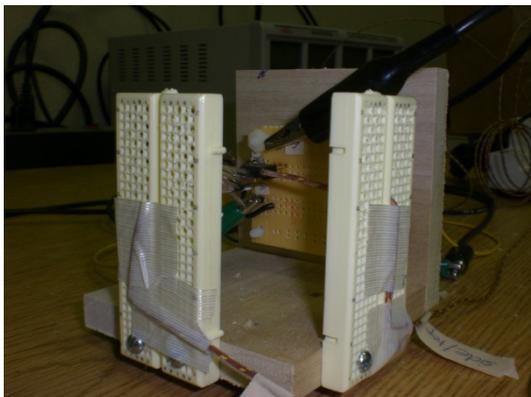


Figure 44: Set-Up Side Mounting View 1

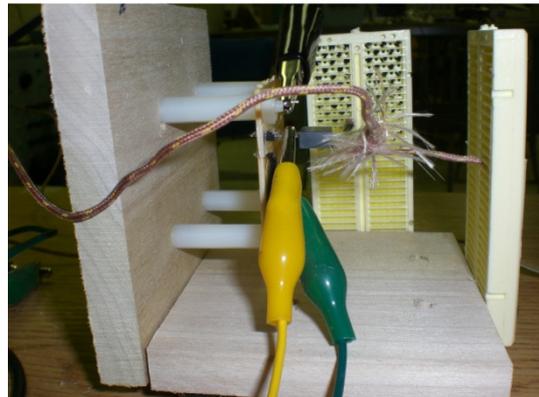


Figure 45: Set-Up Side Mounting View 2

The thermocouples for the temperature measurements changed now to the top and the bottom of the MOSFET. The steady state temperature for these measurements was about 165°C.

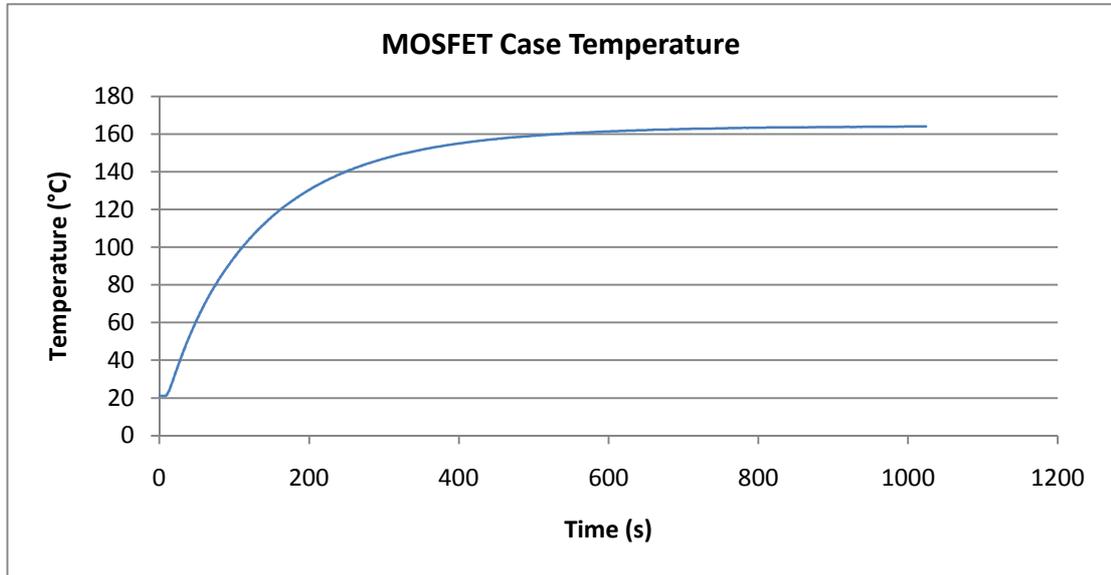


Figure 46: MOSFET Case Temperature (Side Mounting)

The same measurements like for the upright mounting had to be done also for the side mounting. The distances of the thermocouples to the MOSFET were the same, of course.

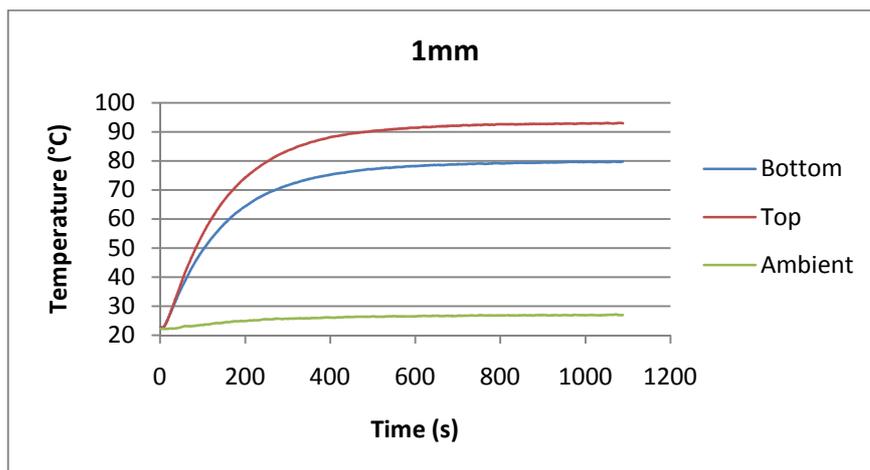


Figure 47: Surrounding Temperature Effects 1mm Distance (Side Mounting)

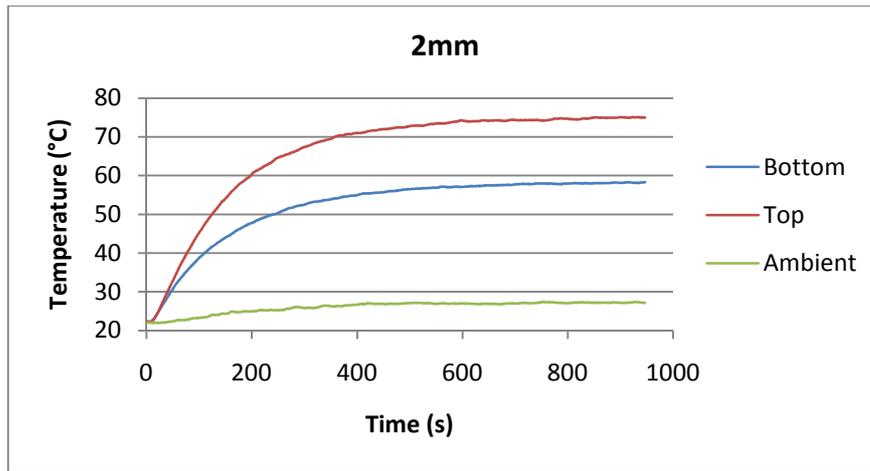


Figure 48: Surrounding Temperature Effects 2mm Distance (Side Mounting)

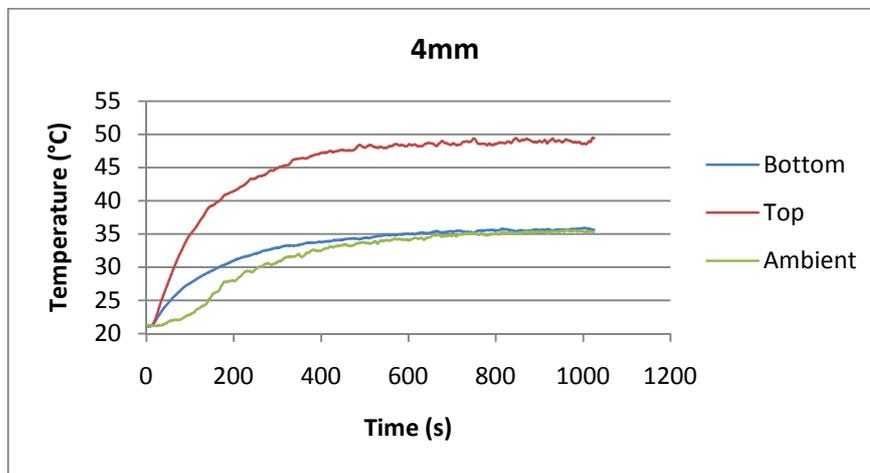


Figure 49: Surrounding Temperature Effects 4mm Distance (Side Mounting)

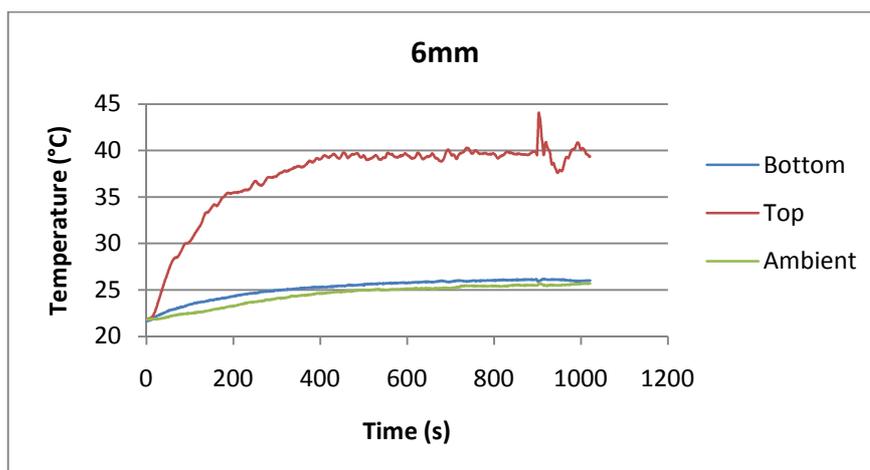


Figure 50: Surrounding Temperature Effects 6mm Distance (Side Mounting)

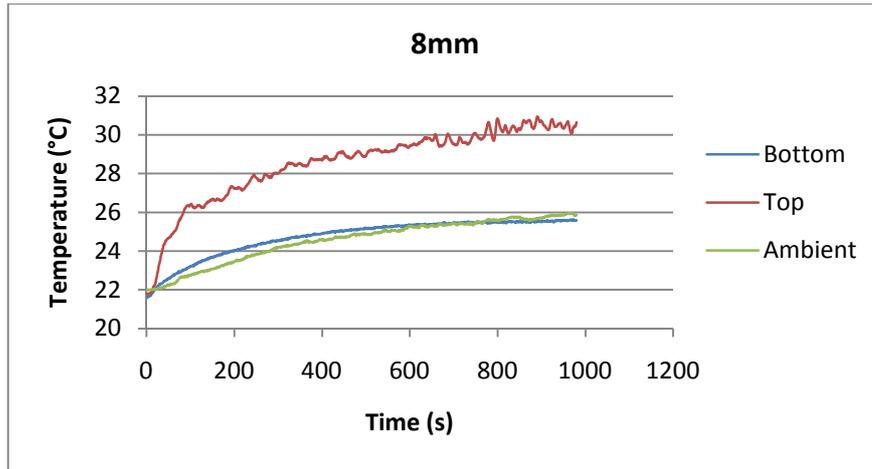


Figure 51: Surrounding Temperature Effects 8mm Distance (Side Mounting)

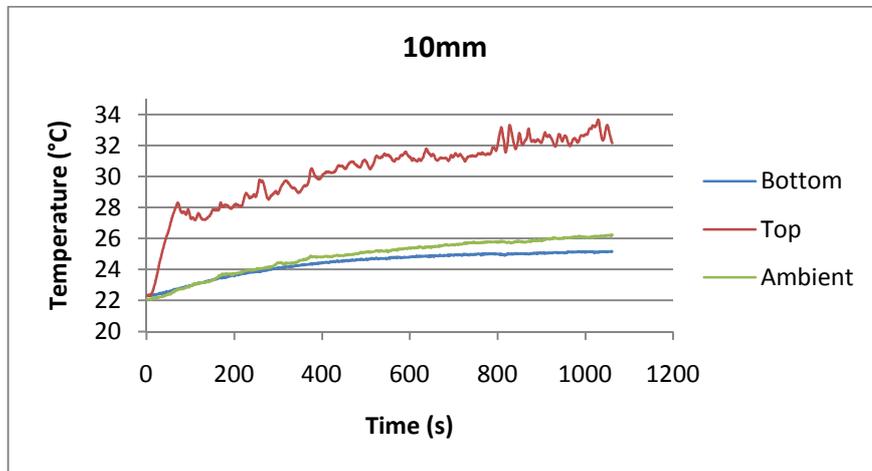


Figure 52: Surrounding Temperature Effects 10mm Distance (Side Mounting)

In this series of measurements you can see a great difference between the top and the bottom temperature. The bottom temperature is already at a distance of 4mm equal to the ambient temperature. Compared to the first measurements, here, much higher temperatures are achieved in the ambience of the MOSFET. Therefore, the mounting of the MOSFET has an influence of the surrounding temperature effects and thus the standards for cooling can vary from the type of mounting.

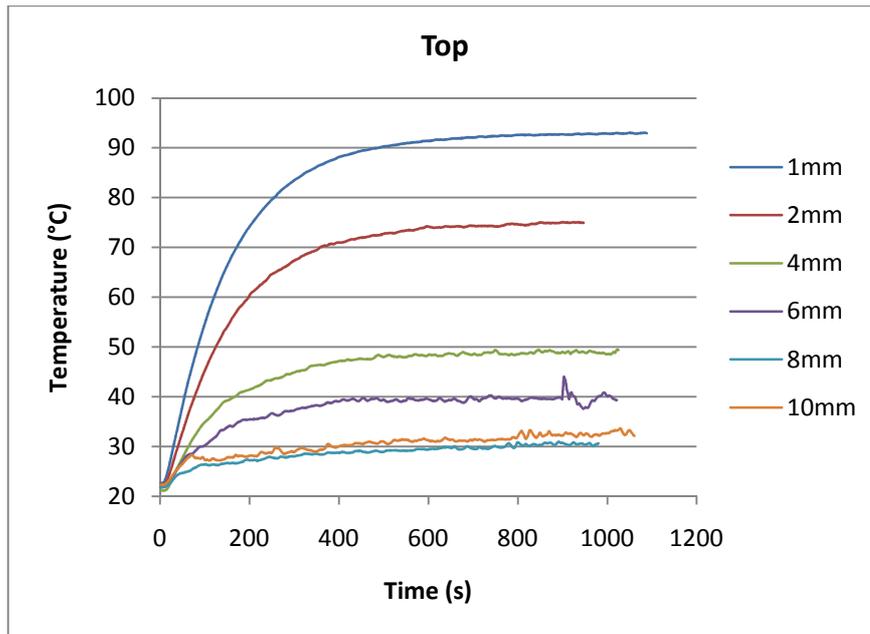


Figure 53: Surrounding Temperature Effects above the MOSFET (Side Mounting)

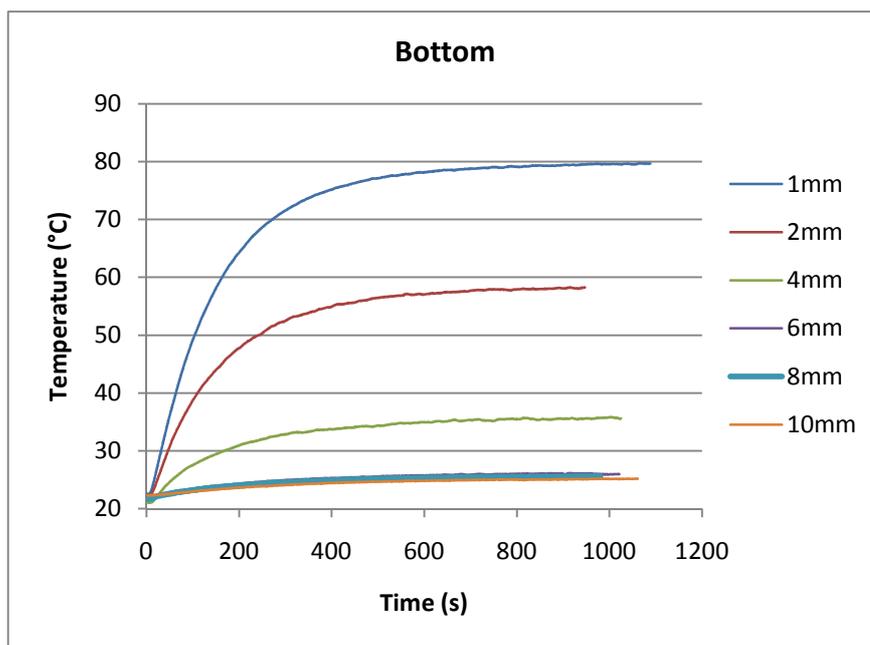


Figure 54: Surrounding Temperature Effects under the MOSFET (Side Mounting)

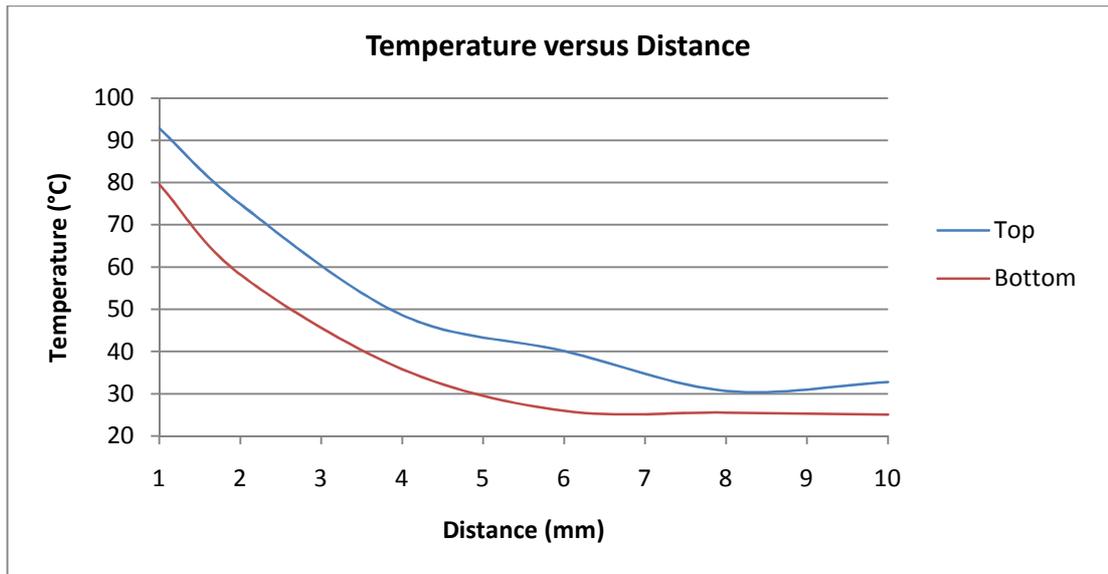


Figure 55: Comparison Temperature versus Distance after 1000s (Side Mounting)

4.2 Measurements with Aluminum Enclosure

The application of Power MOSFETs without any enclosure is very seldom in typical devices, in fact there is a trend to smaller enclosures for electronic circuits. Therefore the next series of measurements were made in an aluminum enclosure. The size of this box was 13.3cm x 7.6cm x 5.4cm. In this box the MOSFET was mounted upright with thermocouples for the front, side and ambient temperature. In contrast to the measurements in the cardboard, the thermocouple for the ambient temperature was here very close above the MOSFET, about 3cm.

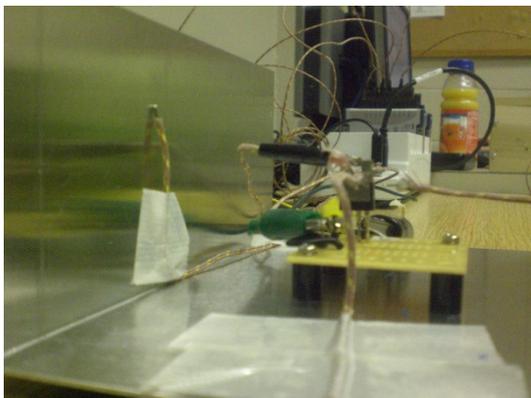


Figure 56: Set-Up in enclosure (opened)



Figure 57: Set-Up in enclosure (closed)

The measurements inside the enclosure were also done with the different distances of 1mm, 2mm, 4mm, 6mm, and 8mm. So the test bed set-up was exactly the same like in the previous measurements, just with another enclosure. The MOSFET case temperature for these measurements was about 180°C.

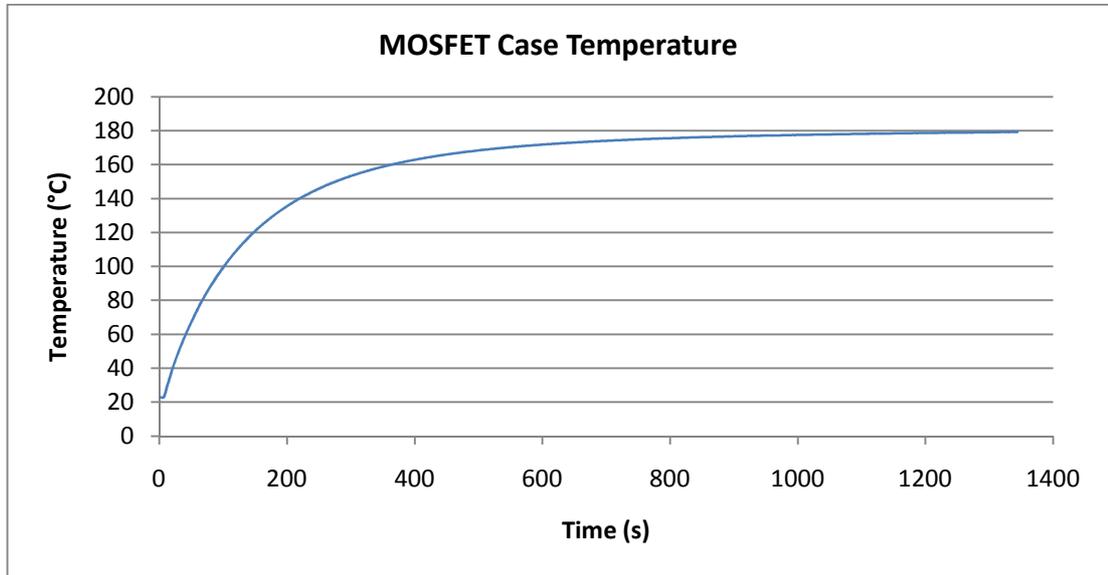


Figure 58: MOSFET Case Temperature (aluminum enclosure)

The results of the measurements inside the enclosure:

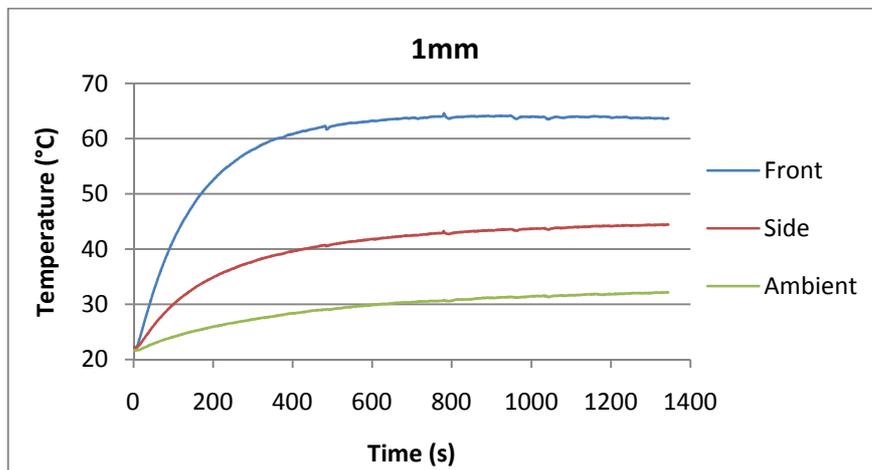


Figure 59: Surrounding Temperature Effects 1mm Distance (Aluminum Enclosure)

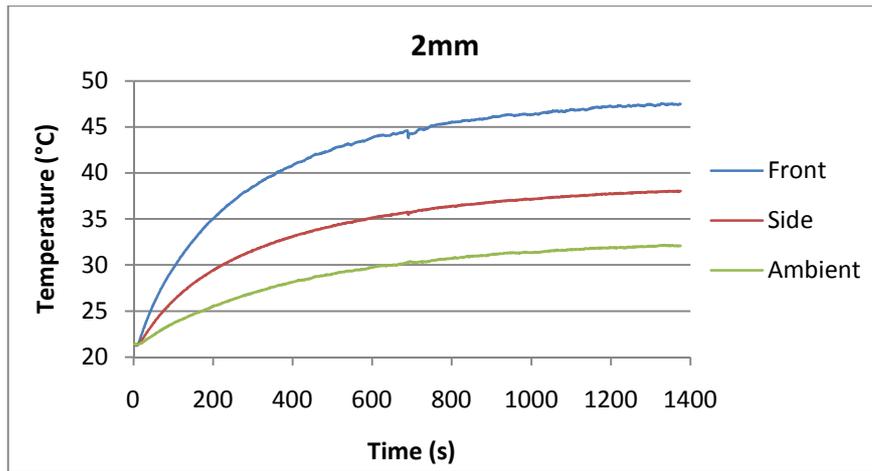


Figure 60: Surrounding Temperature Effects 2mm Distance (Aluminum Enclosure)

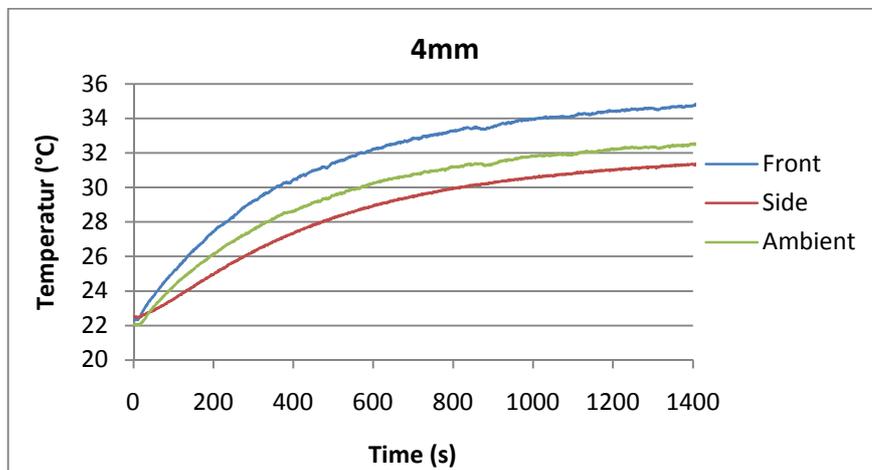


Figure 61: Surrounding Temperature Effects 4mm Distance (Aluminum Enclosure)

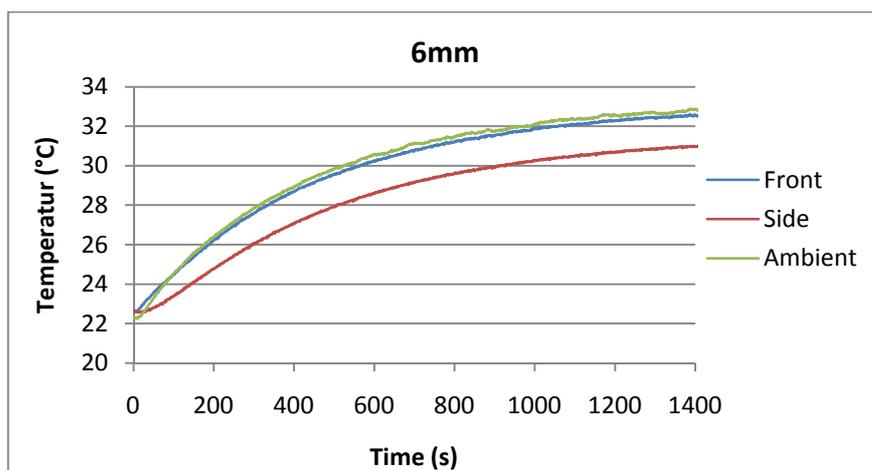


Figure 62: Surrounding Temperature Effects 6mm Distance (Aluminum Enclosure)

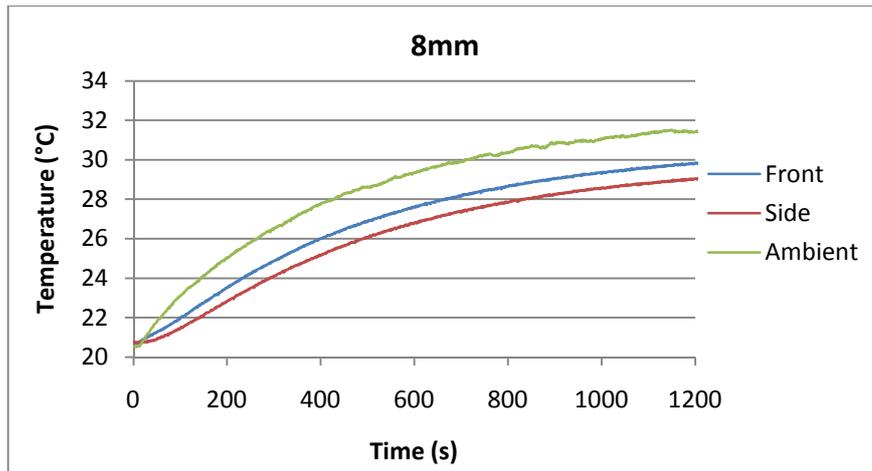


Figure 63: Surrounding Temperature Effects 8mm Distance (Aluminum Enclosure)

For a better overview of the changes of the temperatures according to the distance to the MOSFET, you can find one graph for the front thermocouple and one for the side one.

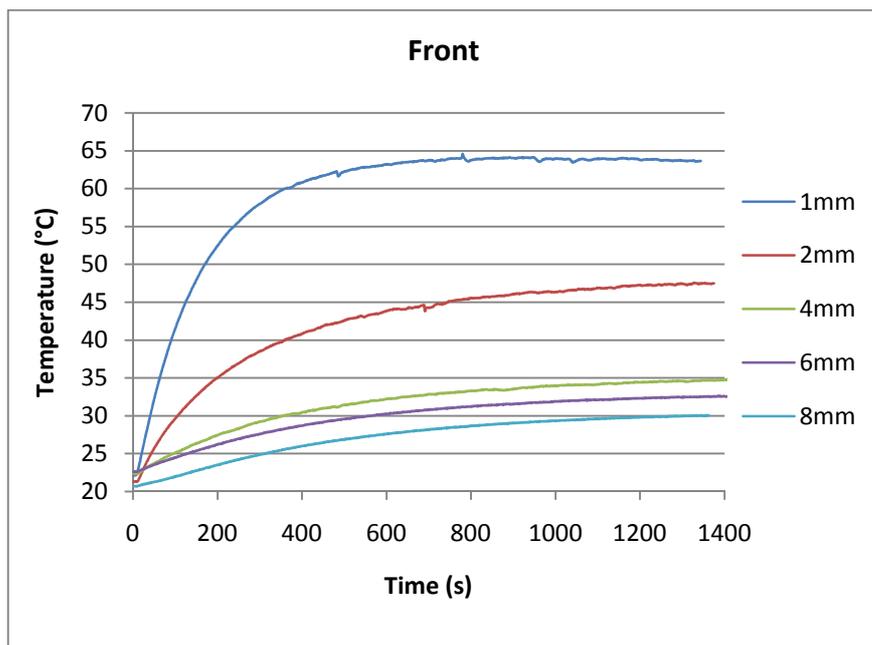


Figure 64: Surrounding Temperature Effects in Front of the MOSFET (Aluminum Enclosure)

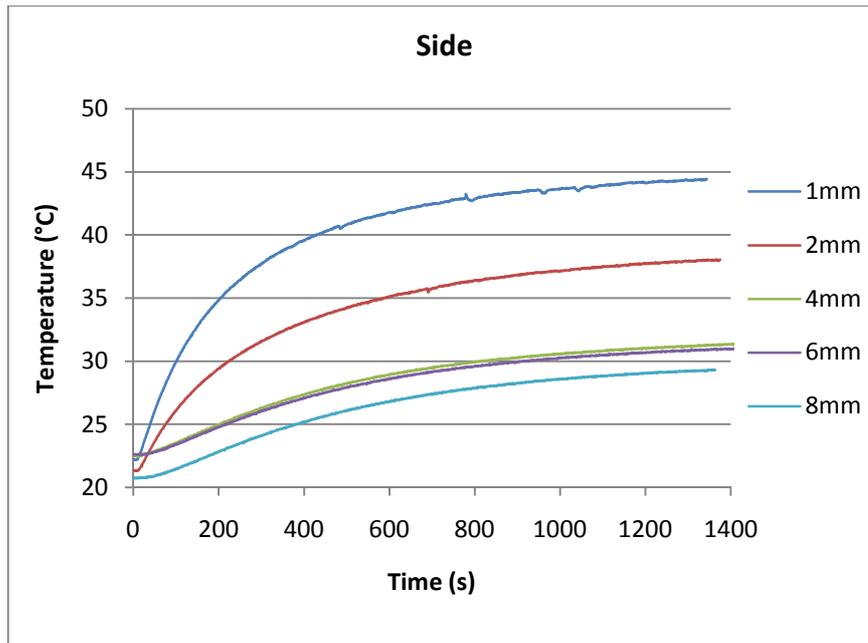


Figure 65: Surrounding Temperature Effects beside the MOSFET (Aluminum Enclosure)

Comparing the results from the measurements with the aluminum enclosure to the results of the measurements without enclosure, you can see a higher temperature achievement inside the enclosure. There is a temperature increase in the front of the MOSFET from 51°C to 64°C at 1mm distance, which is consistent with a raise of about 27%. The temperature beside the MOSFET rises just from 41°C to 44°C, which is consistent with a raise of about 7%. Even at a distance of 8mm there is still a raise of 5°C (20%) in the front of the MOSFET. With these measurements you can see that it is very important to consider not only the mounting of the MOSFET, but also a possible enclosure in which the MOSFET is operated.

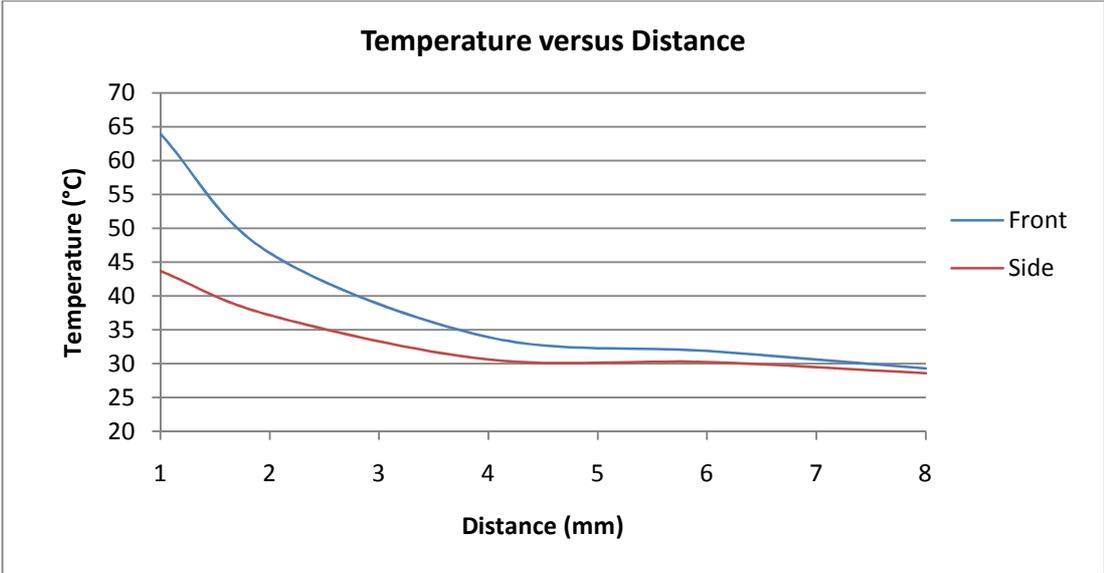


Figure 66: Comparison Temperature versus Distance after 1000s (Aluminum Enclosure)

5 Conclusion

As you can see in the further results of the measurements both the mounting and a possible enclosure affect the heat transfer of an electronic component and consequently also the surrounding temperature effects. Therefore it is very important to define the position and ambience of an electronic component before using it in circuits to detect a necessary cooling.

This thesis contains all necessary information and instructions for future students working on this project. The future work can be done constitutive on the results and information given in this paper. Of course, this paper bases upon the MOSFET power transistor IRLZ14, but the general structure of this paper is the same for all possible electronic components.

The goal for the future student in this project is the actual construction of the test bed based on the information in this paper.

6 *References*

- [1] Yunus A. Çengel, *Heat Transfer: A practical approach*, 2nd ed., New York, 2003
- [2] Robert W. Erickson / Dragan Maksimović, *Fundamentals of Power Electronics*, 2nd ed., 2001
- [3] Heinz Beneking, *Feldeffekttransistoren*, Berlin/Heidelberg, 1973
- [4] Leonce J. Sevin, Jr., *Field-Effect Transistors*, 1965
- [5] Basil L. Cochrun, *Transistor Circuit Engineering*, New York, 1967
- [6] E.J.M. Kendall, *Transistors*, London, 1969
- [7] Carl David Todd, P.E., *Junction Field-Effect Transistors*, New York, 1968
- [8] John D. Lenk, *Handbook of Electronic Components and Circuits*, New Jersey, 1974
- [9] International Rectifier (10/01/2009), [Online], *Power MOSFET Basics*, Available: <http://www.irf.com/technical-info/appnotes/mosfet.pdf>
- [10] Richard C. Dorf, *The Electrical Engineering Handbook*, 2nd ed. 1997
- [11] Phillip A. Laplante, *Comprehensive Dictionary of Electrical Engineering*, Boca Raton, 1999
- [12] Semikron (10/15/2009), [Online], *Leistungs-MOSFET und IGBT*, Available: http://www.semikron.com/internet/webcms/objects/applica_help/d/1_2_1.pdf
- [13] Siliconix (10/03/2009), [Online], *An Introduction to FETs*, Available: application-notes.digchip.com/008/8-12205.pdf
- [14] Fairchild Semiconductors (10/01/2009), [Online], *Introduction to Power MOSFETs and their Applications*, Available: <http://www.fairchildsemi.com/an/AN/AN-558.pdf>

- [15] Fairchild Semiconductors (10/01/2009), [Online], *Power MOSFET Avalanche Guideline*, Available: <http://www.fairchildsemi.com/an/AN/AN-9034.pdf>
- [16] Advanced Power Technology (10/03/2009), [Online], *Power MOSFET Tutorial*, Available: <http://www.microsemi.com/micnotes/APT0403.pdf>
- [17] Power Electronics Technology (10/15/2009), [Online], *Power Management 101: Power MOSFET Characteristics*, Available:
http://powerelectronics.com/power_semiconductors/power_mosfets/power-mosfets-characteristics-0515/
- [18] SMPS Technology Knowledge Base (10/01/2009), [Online], *Power MOSFET Thermal Runaway*, Available: <http://www.smpstech.com/tmos0000.htm>
- [19] Power Management DesignLine (10/15/2009), [Online], *Power MOSFET tutorial, Part 1*, Available:
<http://www.powermanagementdesignline.com/howto/196601551;jsessionid=020CTPL3BF2I3QE1GHOSKHWATMY32JVN>
- [20] Automotive DesignLine (10/15/2009), [Online], *Tech Tutorial: Power MOSFETs: Part 2*, Available:
<http://www.automotivedesignline.com/196603482;jsessionid=5SIZESNJ2NDM3QE1GHPCKHWATMY32JVN?pgno=1>

Appendix A

Absolute Maximum Ratings IRLZ14

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 5.0 V	10	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 5.0 V	7.2	
I_{DM}	Pulsed Drain Current ①	40	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	43	W
	Linear Derating Factor	0.29	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ②	66	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
T_{STG}	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf-in (1.1 N-m)	

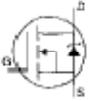
Thermal Resistance IRLZ14

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	3.5	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

Electrical Characteristics IRLZ14 @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.070	—	$^\circ\text{C}$	Reference to 25°C , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	$V_{GS}=5.0\text{V}$, $I_D=6.0\text{A}$ ④
		—	—	0.28		$V_{GS}=4.0\text{V}$, $I_D=5.0\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
g_{fs}	Forward Transconductance	3.5	—	—	S	$V_{DS}=25\text{V}$, $I_D=6.0\text{A}$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS}=60\text{V}$, $V_{GS}=0\text{V}$
		—	—	250		$V_{DS}=48\text{V}$, $V_{GS}=0\text{V}$, $T_J=150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{DS}=10\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10\text{V}$
Q_g	Total Gate Charge	—	—	8.4	nC	$I_D=10\text{A}$
Q_{gs}	Gate-to-Source Charge	—	—	3.5		$V_{DS}=48\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	6.0		$V_{GS}=5.0\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.3	—	ns	$V_{DD}=30\text{V}$
t_r	Rise Time	—	110	—		$I_D=10\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	17	—		$R_G=12\Omega$
t_f	Fall Time	—	26	—		$R_D=2.8\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	400	—	pF	$V_{DS}=0\text{V}$
C_{oss}	Output Capacitance	—	170	—		$V_{DS}=25\text{V}$
C_{riss}	Reverse Transfer Capacitance	—	42	—		$f=1.0\text{MHz}$ See Figure 5

Source-drain Ratings and Characteristics IRLZ14

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	40		
V_{SD}	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}$, $I_S=10\text{A}$, $V_{GS}=0\text{V}$ ②
t_{rr}	Reverse Recovery Time	—	93	130	ns	$T_J=25^\circ\text{C}$, $I_F=10\text{A}$
Q_{rr}	Reverse Recovery Charge	—	0.34	0.65	μC	$di/dt=100\text{A}/\mu\text{s}$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				